

SiT3522

340 to 725 MHz Elite Platform I2C/SPI Programmable Oscillator



Description

The **SiT3522** is an ultra-low jitter, user programmable oscillator which offers the system designer great flexibility and functionality.

The device supports two in-system programming options after powering up at a default, factory programmed startup frequency:

- Any-frequency mode where the clock output can be re-programmed to any frequency between 340 MHz and 725 MHz in 1 Hz steps
- Digitally controlled oscillator (DCO) mode where the clock output can be steered or pulled by up to ± 3200 ppm with 5 to 94 ppt (parts per trillion) resolution.

A user specifies the device's default start-up frequency in the ordering code. User programming of the device is achieved via I²C or SPI. Up to 16 I²C addresses can be specified by the user either as a factory programmable option or via hardware pins, enabling the device to share the I²C with other I²C devices.

The SiT3522 utilizes SiTime's unique DualMEMS[®] temperature sensing and TurboCompensation[®] technology to deliver exceptional dynamic performance

- Resistant to airflow and thermal shock
- Resistant to shock and vibration
- Superior power supply noise rejection

Combined with wide frequency range and user programmability, this device is ideal for telecom, networking and industrial applications that require a variety of frequencies and operate in noisy environment.

Features

- Programmable frequencies (factory or via I²C/SPI) from 340.000001 MHz to 725 MHz
- Digital frequency pulling (DCO) via I²C/SPI
 - Output frequency pulling with perfect pull linearity
 - 13 programmable pull range options to ± 3200 ppm
 - Frequency pull resolution as low as 5 ppt (0.005 ppb)
- 0.21 ps typical integrated phase jitter (12 kHz to 20 MHz)
- Integrated LDO for on-chip power supply noise filtering
- 0.02 ps/mV PSNR
- 40°C to 105°C operating temperature
- LVPECL, LVDS, or HCSL outputs
 - Programmable LVPECL, LVDS Swing
 - LVDS Common Mode Voltage Control
- RoHS and REACH compliant, Pb-free, Halogen-free and Antimony-free

Applications

- Ethernet: 1/10/40/100/400 Gbps
- G.fast and xDSL
- Optical Transport: SONET/SDH, OTN
- Clock and data recovery
- Processor over-clocking
- Low jitter clock generation
- Server, storage, datacenter
- Test and measurement
- Broadcasting

Order samples

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Block Diagram

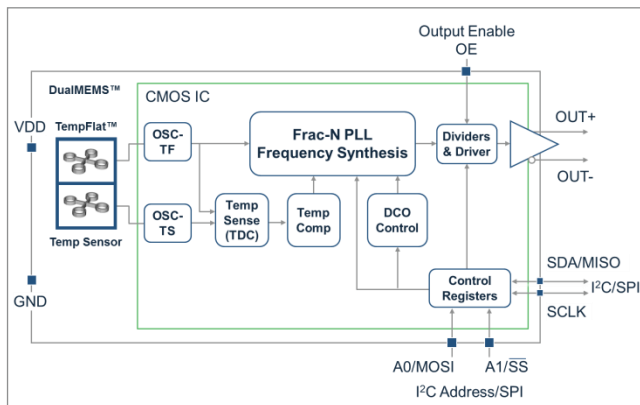


Figure 1. SiT3522 Block Diagram

Package Pinout (10-Lead QFN, 5.0 x 3.2 mm)

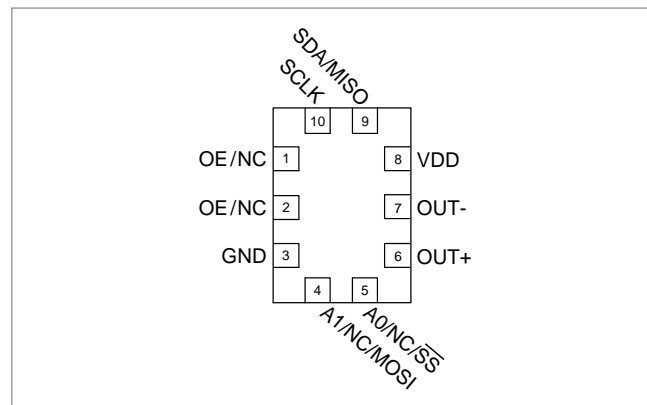


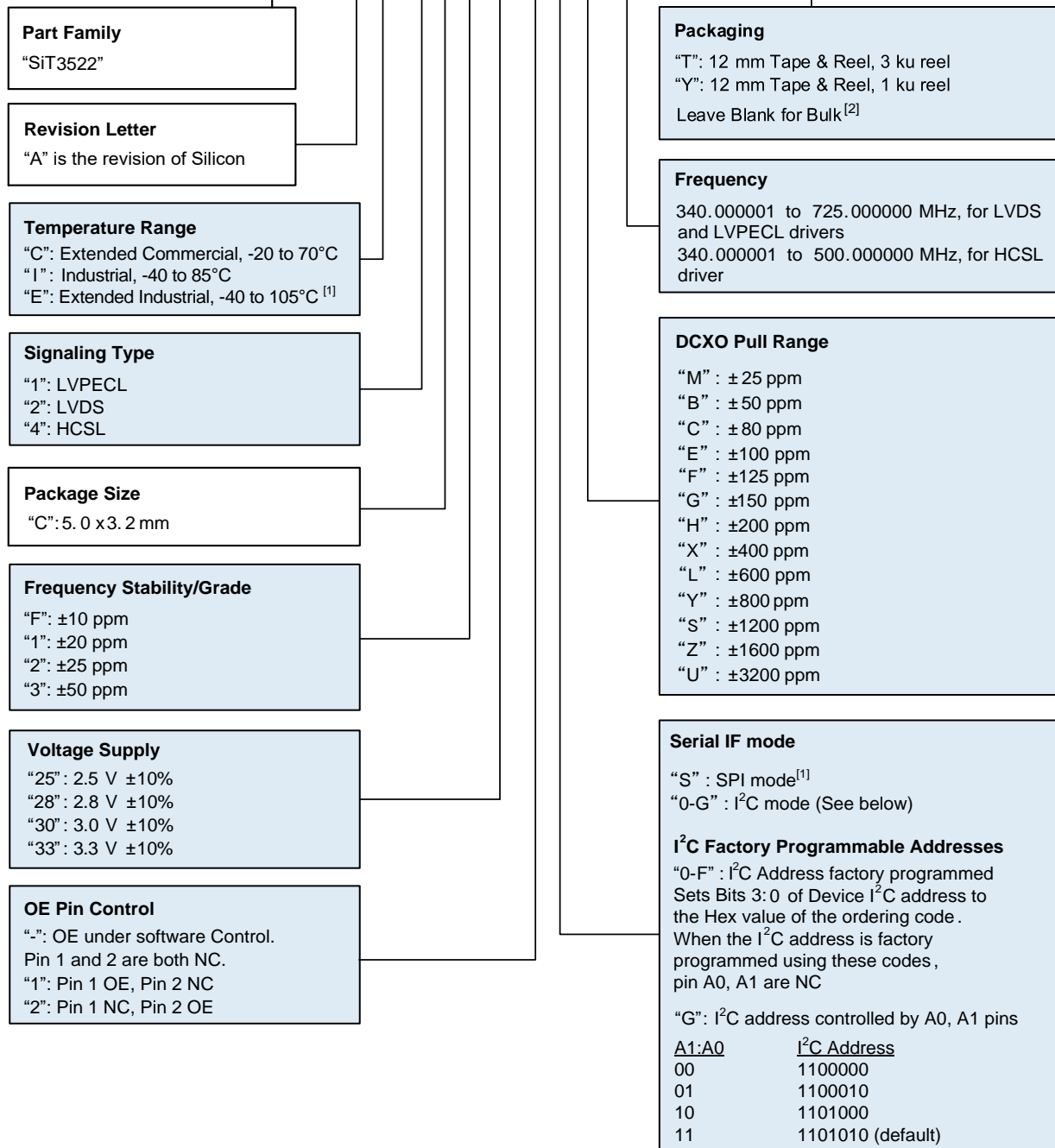
Figure 2. Pin Assignments (Top view)
(Refer to Table 14 for Pin Descriptions)

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Ordering Information

SiT3522 AC-1C1331GG622.080000T



Notes:

- 40 to 105°C option available only for I²C operation.
- Bulk is available for sampling only.

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1 Electrical Characteristics

All Min and Max limits in the Electrical Characteristics tables are specified over temperature and rated operating voltage with standard output terminations shown in the termination diagrams. Typical values are at 25°C and nominal supply voltage.

Table 1. Electrical Characteristics – Common to LVPECL, LVDS and HCSL

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|--|--------------------|------------|------|------------|-----------------|--|
| Frequency Range | | | | | | |
| Output Frequency Range | f | 340.000001 | – | 725.000000 | MHz | LVDS and LVPECL output driver, factory or user programmable, accurate to 6 decimal places |
| | | 340.000001 | – | 500.000000 | MHz | HCSL output driver, factory or user programmable, accurate to 6 decimal places |
| Frequency Stability | | | | | | |
| Frequency Stability | F_stab | -20 | – | +20 | ppm | Inclusive of initial tolerance, operating temperature, rated power supply voltage and load variations |
| | | -20 | – | +20 | ppm | |
| | | -25 | – | +25 | ppm | |
| | | -50 | – | +50 | ppm | |
| First Year Aging | F_1y | – | ±1 | – | ppm | 1 st -year aging at 25°C |
| Temperature Range | | | | | | |
| Operating Temperature Range | T_use | -20 | – | +70 | °C | Extended Commercial |
| | | -40 | – | +85 | °C | Industrial |
| | | -40 | – | +105 | °C | Extended Industrial. Available only for I ² C operation, not SPI. |
| Supply Voltage | | | | | | |
| Supply Voltage | Vdd | 2.97 | 3.3 | 3.63 | V | |
| | | 2.7 | 3.0 | 3.3 | V | |
| | | 2.52 | 2.8 | 3.08 | V | |
| | | 2.25 | 2.5 | 2.75 | V | |
| Input Characteristics – OE Pin | | | | | | |
| Input Voltage High | V _{IH} | 70% | – | – | V _{dd} | OE pin |
| Input Voltage Low | V _{IL} | – | – | 30% | V _{dd} | OE pin |
| Input Pull-up Impedance | Z _{in} | – | 100 | – | kΩ | OE pin, logic high or logic low |
| Output Characteristics | | | | | | |
| Duty Cycle | DC | 45 | – | 55 | % | |
| Startup and Output Enable/Disable Timing | | | | | | |
| Start-up Time | T _{start} | – | – | 3.0 | ms | Measured from the time V _{dd} reaches its rated minimum value |
| Output Enable/Disable Time – Hardware control via OE pin | T _{oe_hw} | – | – | 9.1 | μs | Measured from the time OE pin reaches rated V _{IH} and V _{IL} to the time clock pins reach 90% of swing and high-Z. See Figure 9 and Figure 10 |
| Output Enable/Disable Time – Software control via I ² C/SPI | T _{oe_sw} | – | – | 11.8 | μs | Measured from the time the last byte of command is transmitted via I ² C/SPI (reg1) to the time clock pins reach 90% of swing and high-Z. See Figure 30 and Figure 31 |

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Table 2. Electrical Characteristics – LVPECL Specific

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---------------------------------|------------------------|-------|------------------------|------|---|
| Current Consumption | | | | | | |
| Current Consumption | I _{dd} | – | – | 94 | mA | Excluding Load Termination Current, V _{dd} = 3.3 V or 2.5 V |
| OE Disable Supply Current | I _{OE} | – | – | 63 | mA | OE = Low |
| Output Disable Leakage Current | I _{leak} | – | 0.10 | – | μA | OE = Low |
| Maximum Output Current | I _{driver} | – | – | 30 | mA | Maximum average current drawn from OUT+ or OUT- |
| Output Characteristics | | | | | | |
| Output High Voltage | V _{OH} | V _{dd} - 1.1V | – | V _{dd} - 0.7V | V | See Figure 5 |
| Output Low Voltage | V _{OL} | V _{dd} - 1.9V | – | V _{dd} - 1.5V | V | See Figure 5 |
| Output Differential Voltage Swing | V _{Swing} | 1.2 | 1.6 | 2.0 | V | See Figure 6 |
| Rise/Fall Time | T _r , T _f | – | 225 | 290 | ps | 20% to 80%, see Figure 6 |
| Jitter | | | | | | |
| RMS Phase Jitter (random) – DCO Mode Only | T _{phj} | – | 0.22 | 0.260 | ps | f = 622.08 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V _{dd} levels |
| | | – | 0.075 | 0.085 | ps | f = 622.08, IEEE802.3-2005 10 GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, all V _{dd} levels |
| RMS Phase Jitter (random) – Any-frequency Mode Only | T _{phj} | – | 0.23 | 0.325 | ps | f = 622.08 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V _{dd} levels |
| | | – | 0.09 | 0.095 | ps | f = 622.08, IEEE802.3-2005 10 GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, all V _{dd} levels |
| RMS Period Jitter ^[3] | T _{jitt} | – | 1 | 1.6 | ps | f = 622.08 MHz, V _{dd} = 3.3 V or 2.5 V |

Note:

3. Measured according to JESD65B

Table 3. Electrical Characteristics – LVDS Specific

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---------------------------------|-------|-------|-------|------|---|
| Current Consumption | | | | | | |
| Current Consumption | I _{dd} | – | – | 89 | mA | Excluding Load Termination Current, V _{dd} = 3.3 V or 2.5 V |
| OE Disable Supply Current | I _{OE} | – | – | 67 | mA | OE = Low |
| Output Disable Leakage Current | I _{leak} | – | 0.15 | – | μA | OE = Low |
| Output Characteristics | | | | | | |
| Differential Output Voltage | V _{OD} | 250 | – | 530 | mV | f = 622.08 MHz. See Figure 7 |
| Delta VOD | ΔV _{OD} | – | – | 50 | mV | See Figure 7 |
| Offset Voltage | V _{OS} | 1.125 | – | 1.375 | V | See Figure 7 |
| Delta VOS | ΔV _{OS} | – | – | 50 | mV | See Figure 7 |
| Rise/Fall Time | T _r , T _f | – | 340 | 460 | ps | Measured with 2 pF capacitive loading to GND, 20% to 80%, see Figure 8 |
| Jitter | | | | | | |
| RMS Phase Jitter (random) – DCO Mode Only | T _{phj} | – | 0.21 | 0.255 | ps | f = 622.08 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V _{dd} levels |
| | | – | 0.060 | 0.070 | ps | f = 622.08 MHz, IEEE802.3-2005 10 GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, all V _{dd} levels |
| RMS Phase Jitter (random) – Any-frequency Mode Only | T _{phj} | – | 0.21 | 0.320 | ps | f = 622.08 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V _{dd} levels |
| | | – | 0.070 | 0.80 | ps | f = 622.08 MHz, IEEE802.3-2005 10 GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, all V _{dd} levels |
| RMS Period Jitter ^[4] | T _{jitt} | – | 1 | 1.6 | ps | f = 622.08 MHz, V _{dd} = 3.3 V or 2.5 V |

Note:

4. Measured according to JESD65B.

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Table 4. Electrical Characteristics – HCSL

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|--------------------|-------|-------|-------|------|---|
| Current Consumption | | | | | | |
| Current Consumption | I _{dd} | – | – | 97 | mA | Excluding Load Termination Current, V _{dd} = 3.3 V or 2.5 V |
| OE Disable Supply Current | I _{OE} | – | – | 63 | mA | OE = Low |
| Output Disable Leakage Current | I _{leak} | – | 0.15 | – | μA | OE = Low |
| Output Characteristics | | | | | | |
| Output High Voltage | VOH | 0.60 | – | 0.90 | V | See Figure 5 |
| Output Low Voltage | VOL | -0.10 | – | 0.10 | V | See Figure 5 |
| Output Differential Voltage Swing | V _{Swing} | 1.2 | 1.4 | 1.8 | V | See Figure 6 |
| Rise/Fall Time | Tr, Tf | – | 360 | 470 | ps | Measured with 2 pF capacitive loading to GND, 20% to 80%, see Figure 6 |
| Jitter | | | | | | |
| RMS Phase Jitter (random) – DCO mode only | T _{phj} | – | 0.215 | 0.250 | ps | f = 622.08 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V _{dd} levels |
| | | – | 0.065 | 0.075 | ps | f = 622.08 MHz, IEEE802.3-2005 10 GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, all V _{dd} levels |
| RMS Phase Jitter (random) – Any-frequency mode only | T _{phj} | – | 0.240 | 0.310 | ps | f = 622.08 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V _{dd} levels |
| | | – | 0.70 | 0.080 | ps | f = 622.08 MHz, IEEE802.3-2005 10 GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, all V _{dd} levels |
| RMS Period Jitter ^[5] | T _{jitt} | – | 1.0 | 1.6 | ps | f = 622.08 MHz, V _{dd} = 3.3 V or 2.5 V |

Note:

5. Measured according to JESD65B.

Table 5. I²C Electrical Characteristics – SCLK, SDA, 1 MHz SCLK, 255 Ohm, 550 pF (Max I²C Bus Load)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|--------------------------------------|-----------------|------|------|------|-----------------|--|
| Input Voltage Low | VIL | – | – | 30% | V _{dd} | |
| Input Voltage High | VIH | 70% | – | – | V _{dd} | |
| Output Voltage Low | VOL | – | – | 0.4 | V | |
| Input Leakage current ^[6] | I _L | 0.5 | – | 24 | μA | 0.1 V _{DD} < V _{OUT} < 0.9 V _{DD} |
| Input Capacitance | C _{IN} | – | – | 5 | pF | |

Note:

 6. Including leakage current from 160 kOhm pull resistor at typical condition to V_{DD}.

Table 6. SPI Electrical Characteristics – SCLK, MOSI, \overline{SS} , MISO

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|--|-----------------|------|------|------|-----------------|--|
| Input Pins – SCLK, MOSI, \overline{SS} | | | | | | |
| Input Voltage Low | VIL | – | – | 10% | V _{dd} | |
| Input Voltage High | VIH | 90% | – | – | V _{dd} | |
| Input Capacitance | C _{IN} | – | – | 5 | pF | |
| Output Pin – MISO | | | | | | |
| Output Voltage High | VOH | 90% | – | – | V _{dd} | I _{OH} = 2.2 mA (V _{dd} = 2.5 V) |
| Output Voltage Low | VOL | – | – | 10% | V _{dd} | I _{OL} = 2.7 mA (V _{dd} = 2.5 V) |
| Leakage in high impedance mode | I _L | 5.5 | – | 24 | μA | 0.1 V _{dd} < V _{OUT} < 0.9 V _{dd} |

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Table 7. Typical Phase Noise: Default start-up or reprogrammed frequency in DCO mode – LVDS output clock

| Frequency Offsets | Output Frequency Phase Noise (dBc/Hz) | |
|-------------------|---------------------------------------|---------|
| | 622.08 MHz | 725 MHz |
| 100 Hz | -86.7 | -85.1 |
| 1 kHz | -111.7 | -109.1 |
| 10 kHz | -119.6 | -117.3 |
| 100 kHz | -121.2 | -119.5 |
| 1 MHz | -137.5 | -133.8 |
| 10 MHz | -150.6 | -148.8 |
| 20 MHz | -152.4 | -150.9 |

Table 8. Typical Phase Noise: Reprogrammed frequency in any-frequency Mode – LVDS output clock

| Frequency Offsets | Output Frequency Phase Noise (dBc/Hz) | |
|-------------------|---------------------------------------|---------|
| | 622.08 MHz | 725 MHz |
| 100 Hz | -86.7 | -85.1 |
| 1 kHz | -111.6 | -109.2 |
| 10 kHz | -120.5 | -117.2 |
| 100 kHz | -123.3 | -119.4 |
| 1 MHz | -135.8 | -134.6 |
| 10 MHz | -149.7 | -148.9 |
| 20 MHz | -152.2 | -150.9 |

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Table 9. Absolute Maximum

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

| Parameter | Min. | Max. | Unit |
|---|------|-------------|------|
| Continuous Power Supply Voltage Range (Vdd) | -0.5 | 4.0 | V |
| Input Voltage, Maximum (any input pin) | – | Vdd + 0.3 V | V |
| Input Voltage, Minimum (any input pin) | -0.3 | – | V |
| Storage Temperature | -65 | 150 | °C |
| Maximum Junction Temperature | – | 135 | °C |
| Soldering Temperature ^[7] (follow standard Pb-free soldering guidelines) | – | 260 | °C |

Note:

7. Exceeding this temperature for an extended period of time may damage the device.

Table 10. Thermal Consideration^[8]

| Package | θ_{JA} , 4 Layer Board (°C/W) | θ_{JC} , Bottom (°C/W) |
|--------------|--------------------------------------|-------------------------------|
| 5032, 10-pin | 55 ^[9] | 20 |

Note:

8. Refer to JESD51 for θ_{JA} and θ_{JC} definitions, and reference layout used to determine the θ_{JA} and θ_{JC} values in the above table.

9. Value for θ_{JA} assumes the center pad is soldered down.

Table 11. Maximum Operating Junction Temperature^[10]

| Max Operating Temperature(ambient) | Maximum Operating Junction Temperature |
|------------------------------------|--|
| 70°C | 95°C |
| 85°C | 110°C |
| 105°C | 130°C |

Note:

10. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

Table 12. Environmental Compliance

| Parameter | Test Conditions | Value | Unit |
|--|---------------------------|--------|------|
| Mechanical Shock Resistance | MIL-STD-883F, Method 2002 | 10,000 | g |
| Mechanical Vibration Resistance | MIL-STD-883F, Method 2007 | 70 | g |
| Soldering Temperature (follow standard Pb free soldering guidelines) | MIL-STD-883F, Method 2003 | 260 | °C |
| Moisture Sensitivity Level | MSL1 @ 260°C | – | – |
| Electrostatic Discharge (HBM) | HBM, JESD22-A114 | 2,000 | V |
| Charge-Device Model ESD Protection | JESD220C101 | 750 | V |
| Latch-up Tolerance | JESD78 Compliant | | |

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2 Device Configurations and Pin-outs

Table 13. Device Configurations

| Programming Interface | Addressing Mode | Pin 4 | Pin 5 | Pin 9 | Pin 10 |
|-----------------------|-----------------|-------|-------|-------|--------|
| I ² C | Pin controlled | A1 | A0 | SDA | SCLK |
| | Software | NC | NC | SDA | SCLK |
| SPI | – | MOSI | SS | MISO | SCLK |

Pin-out Top Views (10-Lead QFN, 5.0mm x 3.2mm)

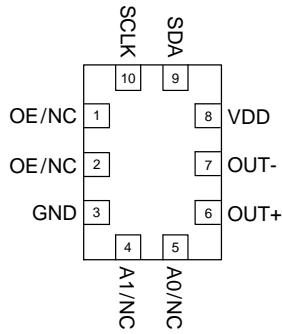


Figure 3. I²C Mode

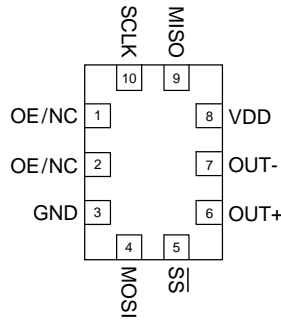


Figure 4. SPI Mode

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Table 14. Pin Description

| Pin | Symbol | I/O | Internal Pull-up/ Pull Down Resistor | Function |
|-----|-----------------|------------|---|---|
| 1 | OE | OE | 100 kΩ Pull-Up | Pin 1 and Pin 2 functions are set by the ordering code in Ordering Information Table . If Software OE mode is selected in Ordering Table, both pin 1 and pin 2 are NC. H ^[11] : Specified frequency output L: Output Driver is disabled: OUT- = High-Z OUT+ = High-Z |
| | NC | No Connect | | No Connect |
| 2 | OE | | 100 kΩ Pull-Up | Pin 1 and Pin 2 functions are set by the ordering code in Ordering Information Table . If Software OE mode is selected in Ordering Table, both pin 1 and pin 2 are NC. H ^[11] : Specified frequency output L: Output Driver is disabled: OUT- = High-Z OUT+ = High-Z |
| | NC | No Connect | | No Connect |
| 3 | GND | Ground | | Connect to ground |
| 4 | A1 | Input | 100 kΩ Pull-Up | I ² C Address Select, Most Significant Bit (MSB) A1 A0 I ² C Address 0 0 1100000 0 1 1100010 1 0 1101000 1 1 1101010 (Default) |
| | NC | No Connect | | No Connect. I ² C Address is factory set to one of the 16 available addresses shown in Table 27 and also on the Ordering Information Table . |
| | MOSI | Input | 100 kΩ Pull-Up | SPI serial data input |
| 5 | A0 | Input | 100 kΩ Pull-Up | I ² C Address Select, Least Significant Bit (LSB) A1 A0 I ² C Address 0 0 1100000 0 1 1100010 1 0 1101000 1 1 1101010 (Default) |
| | NC | No Connect | | No Connect. I ² C Address is factory set to one of the 16 available addresses shown in Table 27 and also on the Ordering Information Table . |
| | \overline{SS} | Input | 100 kΩ Pull-Up | SPI Chip select, active low |
| 6 | OUT+ | Output | | Oscillator output |
| 7 | OUT- | Output | | Complementary oscillator output |
| 8 | VDD | Power | | Connect to VDD ^[12] |
| 9 | SDA | Input | 200 kΩ Pull-Up | I ² C serial data input |
| | MISO | Output | 200 kΩ Pull-Up | SPI serial data output |
| 10 | SCLK | Input | 200 kΩ Pull-Up | I ² C/SPI serial clock input |

Notes:

- In OE mode for noisy environments, a pull-up resistor of 10 kΩ or less is recommended if pin 1 is not externally driven. If OE pin needs to be left floating, use the NC option.
- 0.1 μF capacitor in parallel with a 10 μF capacitor are required between VDD and GND.

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3 Waveform Diagrams

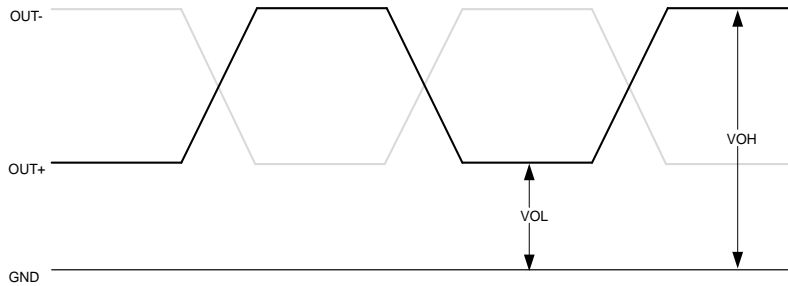


Figure 5. LVPECL, HCSL Voltage Levels per Differential Pin (i.e. OUT+, or OUT-)

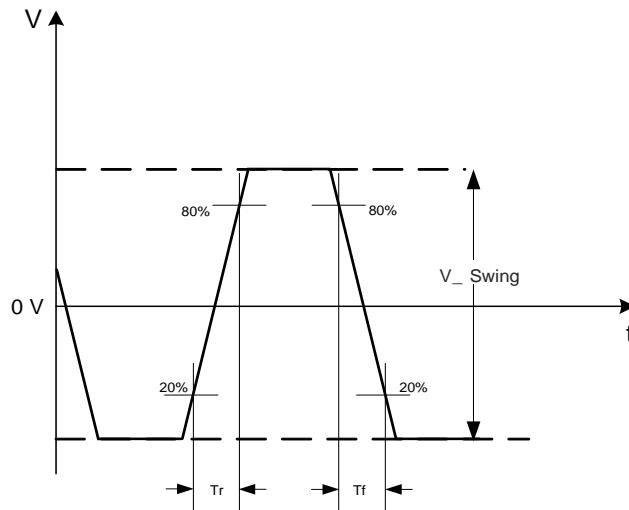


Figure 6. LVPECL, HCSL Voltage Levels Across Differential Pair (i.e. OUT+ minus OUT-)

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Waveform Diagrams (continued)

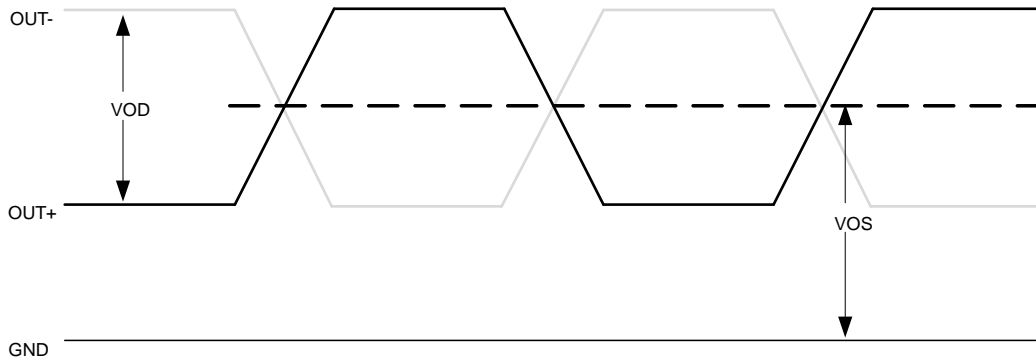


Figure 7. LVDS Voltage Levels per Differential Pin (i.e. OUT+, or OUT-)

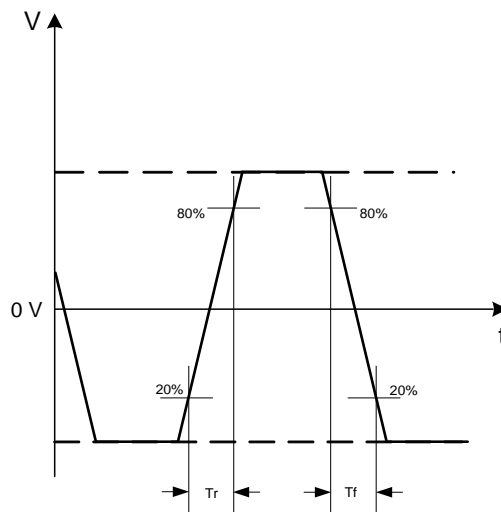


Figure 8. LVDS Differential Waveform (i.e. OUT+ minus OUT-)

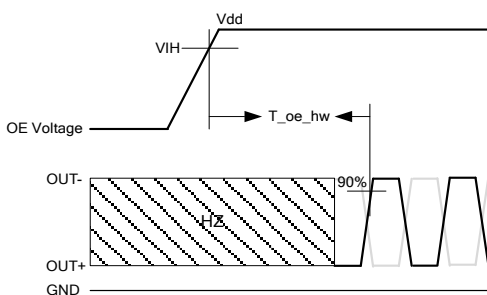


Figure 9. Hardware OE Enable Timing

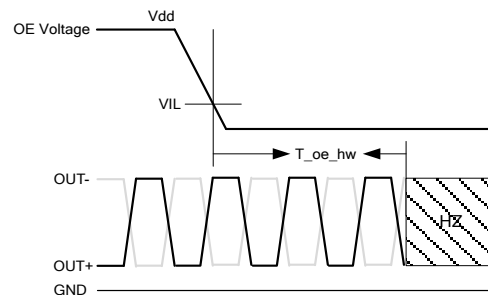


Figure 10. Hardware OE Disable Timing

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4 Termination Diagrams

4.1. LVPECL

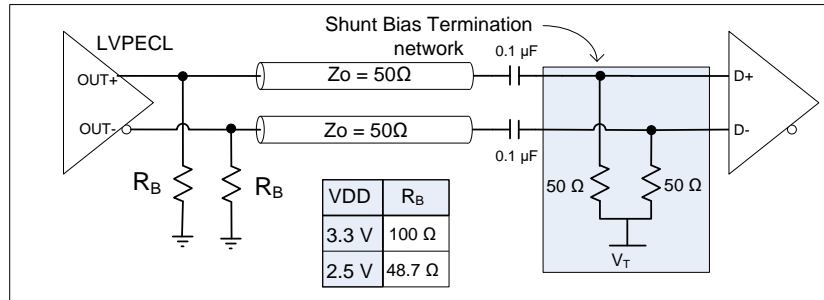


Figure 11. LVPECL with AC-coupled Termination

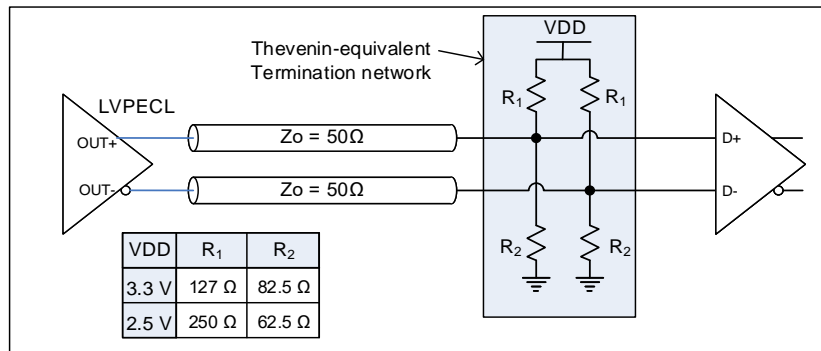


Figure 12. LVPECL DC-coupled Load Termination with Thevenin Equivalent Network

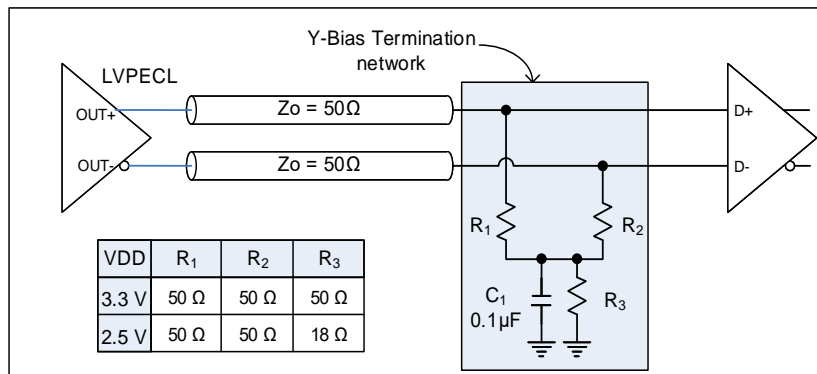


Figure 13. LVPECL with Y-Bias Termination

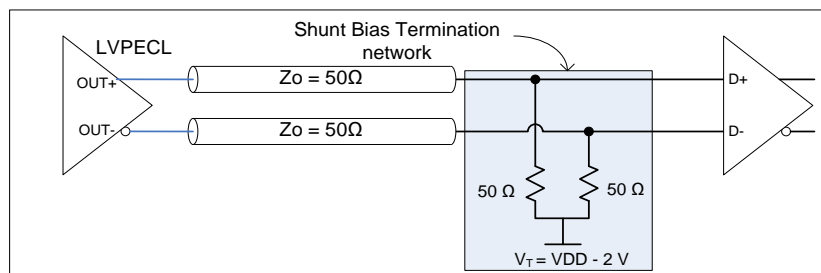


Figure 14. LVPECL with DC-coupled Parallel Shunt Load Termination

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Termination Diagrams (continued)

4.2. LVDS

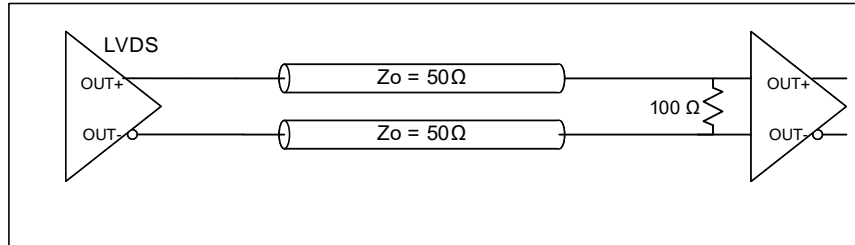


Figure 15. LVDS single DC Termination at the Load

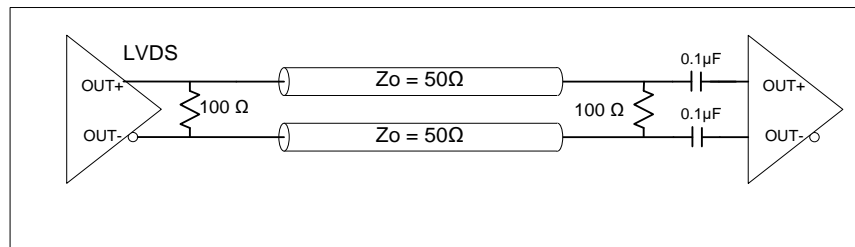


Figure 16. LVDS Double AC Termination with Capacitor Close to the Load

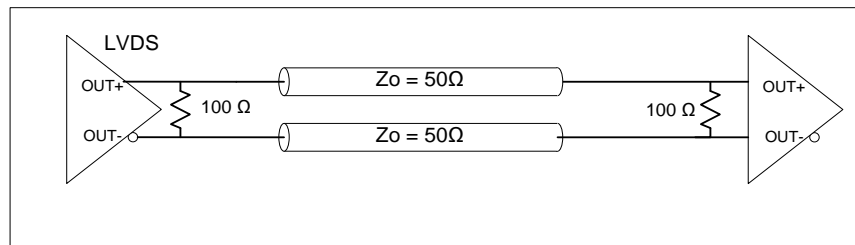


Figure 17. LVDS Double DC Termination

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Termination Diagrams (continued)

4.3. HCSL

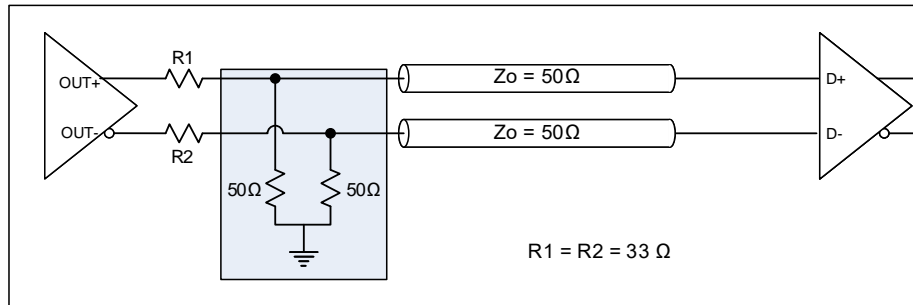


Figure 18. HCSL Interface Termination

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5 Test Circuit Diagrams

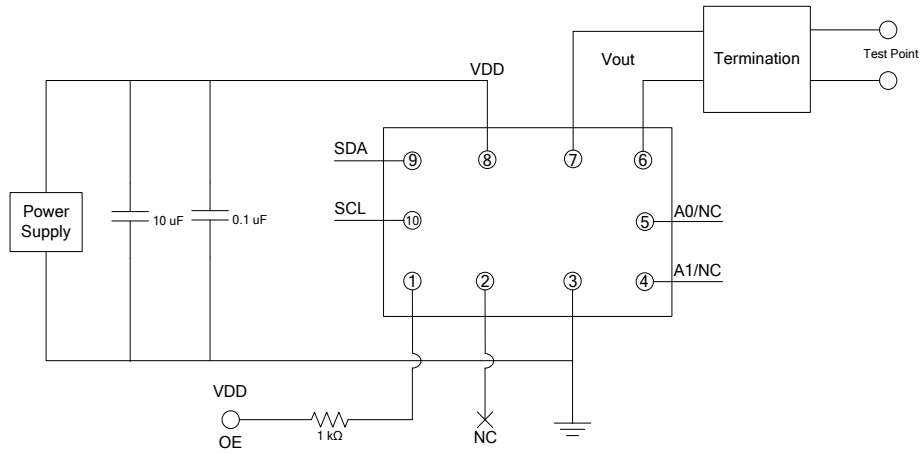


Figure 19. Test Circuit (I²C mode and OE Function for Pin 1)

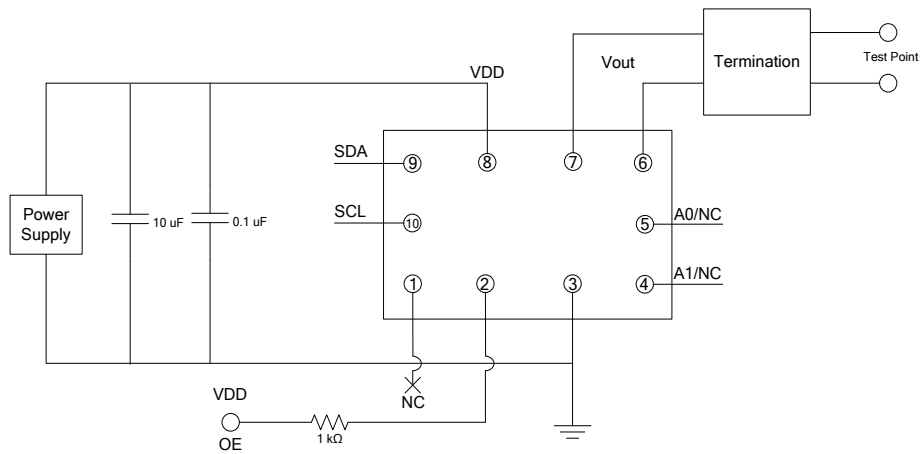


Figure 20. Test Circuit (I²C mode and OE Function for Pin 2)

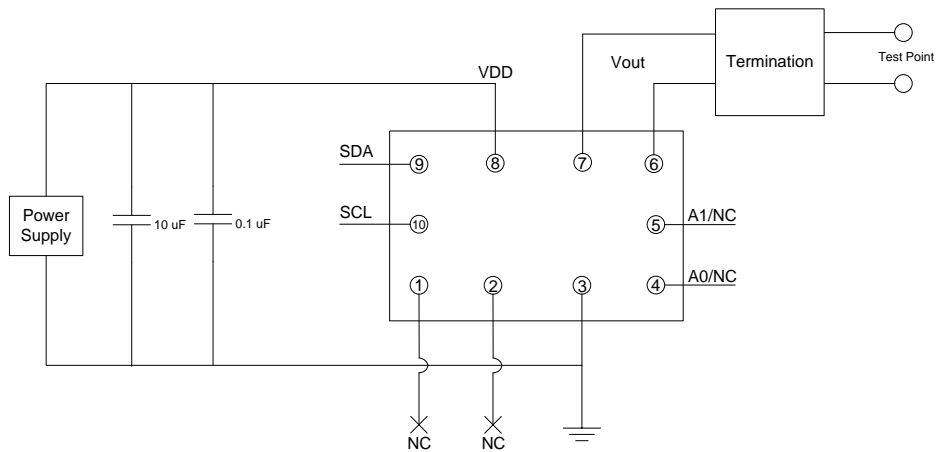


Figure 21. Test Circuit (I²C mode and NC Function for both Pin1 and Pin2)

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Test Circuit Diagrams (continued)

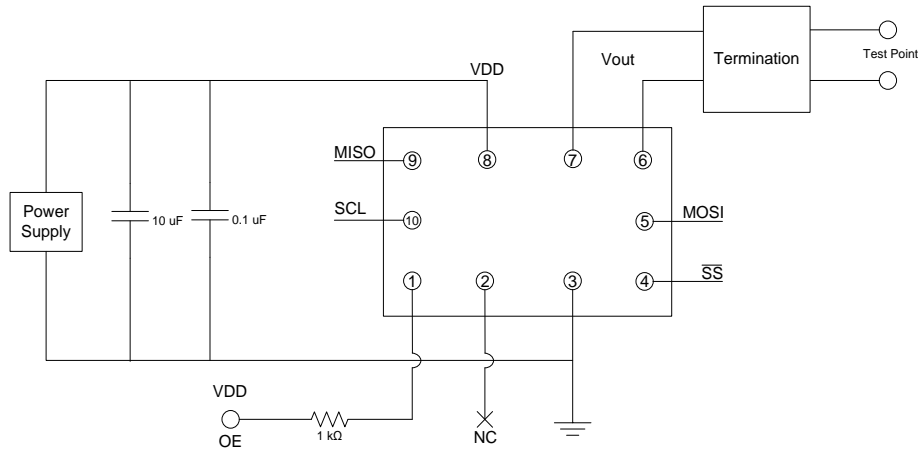


Figure 22. Test Circuit (SPI mode and OE Function for Pin 1)

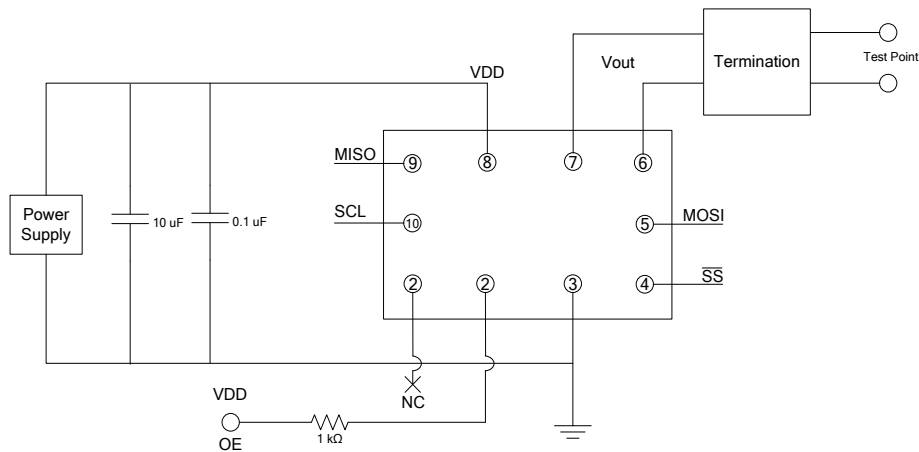


Figure 23. Test Circuit (SPI mode and OE Function for Pin 2)

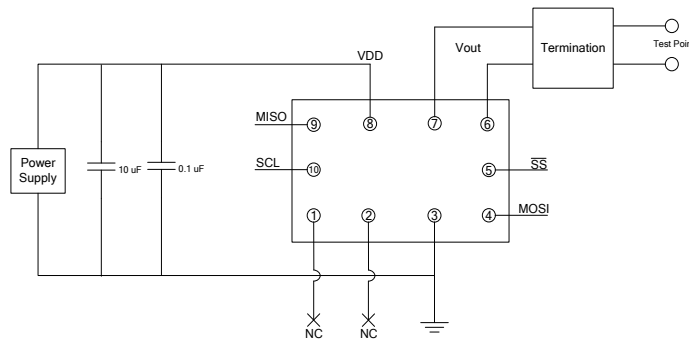


Figure 24. Test Circuit (SPI mode and NC Function for both Pin1 and Pin2)

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6 Architecture Overview

Based on SiTime's innovative Elite Platform®, the SiT3522 delivers exceptional dynamic performance, i.e. resilience to environmental stressors such as shock, vibration and fast temperature transients. Underpinning the Elite platform are SiTime's unique DualMEMS temperature sensing architecture and TurboCompensation technology, illustrated in [Figure 1](#).

DualMEMS is a noiseless temperature sensing scheme. It consists of two MEMS resonators fabricated on the same die substrate. The TempFlat resonator is designed with a flat frequency characteristic over temperature whereas the temperature sensing resonator is by design sensitive to temperature changes. The ratio of frequencies between these two resonators provides an accurate reading of the resonator temperature with 30 μ K resolution.

By placing the two MEMS resonators on the same die, this temperature sensing scheme eliminates the thermal lag and gradients between the resonator and the temperature sensor, an inherent weakness of the legacy quartz TCXOs.

The DualMEMS temperature sensor is then combined with a state-of-the-art temperature compensation circuit in the CMOS IC. The TurboCompensation design, with >100 Hz compensation bandwidth, achieves dynamic frequency stability that is far superior to any quartz devices. The 7th order compensation algorithm enables additional optimization of frequency stability and frequency slope over temperature within any specific temperature range of choice for a given system design.

The Elite platform also incorporates a high resolution, low noise frequency synthesizer along with the industry standard I²C and/or SPI bus. This unique combination enables system designers to digitally control the output frequency in steps as low as 5 ppt (parts per trillion) and over a wide frequency range from 1 MHz to 340 MHz.

For more information regarding the Elite platform and its benefits please visit:

- [SiTime's breakthroughs](#) section
- TechPaper: [DualMEMS Temperature Sensing Technology](#)
- TechPaper: [DualMEMS Resonator TDC](#)

7 Functional Overview

The SiT3522 is designed for maximum frequency flexibility with an array of factory programmable options, enabling system designers to configure this precision device for optimal performance in a given application.

7.1. User Programming Interface

The SiT3522 supports either I²C or SPI interface (slave only) as a factory programmable option via the ordering codes. For I²C, the user has the option of using one of the four default addresses selectable with two address pins (A0, A1) or specifying one of the sixteen factory programmed addresses. Refer to [I²C/SPI Device Address Modes](#) section for details.

Table 15. Programming Interface Ordering Codes

| Programming Interface | Addressing Mode | Ordering Code |
|-----------------------|-------------------------|---------------|
| I ² C | 2 address pins – A0, A1 | "G" |
| | Factory programmed | "0-F" |
| SPI | Chip select pin | "S" |

7.2. Start-up output frequency and signaling types

The SiT3522 is shipped with a default start-up frequency between 1 MHz to 340 MHz in steps of 1 Hz that a user specifies in the ordering code.

A user can also specify one of the three differential signaling types in the ordering code.

Table 16. Output Format Ordering Codes

| Output Format | Ordering Code |
|---------------|---------------|
| LVPECL | "1" |
| LVDS | "2" |
| HCSL | "4" |

7.3. In-system programmable options

The SiT3522 enables software control of the following features via I²C/SPI:

- **Any-frequency feature:** Output frequency that can be re-programmed to any value between 1 MHz and 340 MHz in 1 Hz steps
- **DCO feature:** Output frequency that can be steered (pulled) by up to ± 3200 ppm with 5 to 94 ppt resolution.
- **Software OE feature:** Enabling or disabling of the output driver

Refer to [Chapter 9](#) for programming details.

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8 In-system Programmable Functional Description

Figure 25 shows hi-level block diagram of In-system programmable oscillator showing user accessible and non-user-accessible circuit blocks.

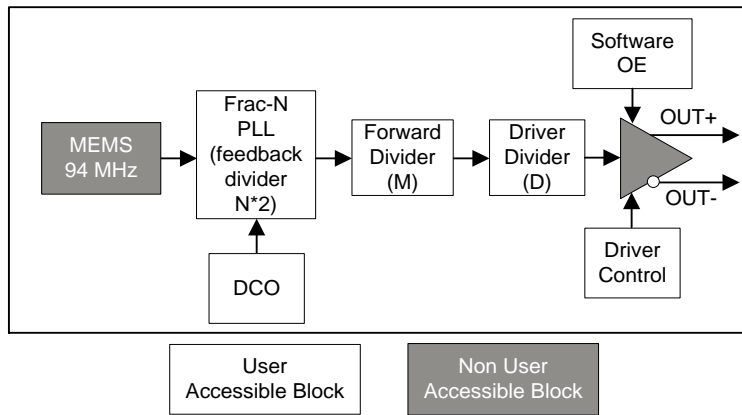


Figure 25. In-system Programmable Oscillator Block Diagram

8.1. Any-frequency function

The any-frequency feature allows users to re-program the device output to a new frequency between 340.000001 MHz to 725 MHz and optimize output driver according to the given new frequency after power-up through the I²C or SPI interface. Device output frequency is defined by a combination of Frac-N PLL feedback divider (N), forward divider (M) and driver divider (D).

Equation 1: Output frequency,

$$F_{out} = \frac{94 \text{ MHz} * N * 2}{D * M}$$

Table 17 is showing unsupported any-frequency Frequencies.

Table 17. List of Unsupported Frequencies

| Unsupported Frequency Range (MHz) | |
|-----------------------------------|----------|
| Min. | Max. |
| 600.4250 | 615.0001 |

To re-program device to the desired output frequency, user should calculate the most appropriate N, M and D dividers combination. For a given output frequency, the choice of dividers combination must fall within the allowable ranges (See the Table 18).

Calculation of the appropriate N, M, D values and selection of proper Driver Control values consist of the following steps. Throughout these steps, and example using LVPECL 622.08 MHz output frequency will be used.

Table 18. Any-frequency user-accessible blocks

| Block Name | Available values | Register Name | Register Address |
|----------------|----------------------|--------------------------|--|
| N | 13.08511 to 15.96875 | N_reg [31:0] | 0x03[15:0] = N_reg[31:16] 0x04[15:0] = N_reg[15:0] |
| M (D = 2) | 2 to 8191 | M_reg [12:0] | 0x05[15:3] = M_reg[12:0] |
| M (D = 1) | 3, 5, 7 | M_reg [12:0] | 0x05[15:3] = M_reg[12:0] |
| D | 1-2 | D_reg[0] | 0x06[3] = D_reg[0] |
| Driver Control | 0 to 63 | Driver Control Reg [5:0] | 0x05[2:0] = Driver Control Reg[5:3] 0x06[2:0] = Driver Control Reg[2:0] |

Step 1: N and M dividers value calculation for D = 2

Find the lowest allowed M value for D = 2 which gives N value (see Equation 2) within allowed Frac-N PLL feedback divider range (see Table 18):

Equation 2:

$$N = \frac{F_{out} * D * M}{94 \text{ MHz} * 2} = \frac{F_{out} * D * M}{188 \text{ MHz}}$$

Top part of Table 19 below shows implementation of this step for the 622.08 MHz output frequency example. The combination satisfying above conditions is highlighted in blue.

Step 2: N and M dividers value calculation for D = 1

Find the lowest allowed M value for D = 1 which gives N value (see Equation 2) within allowed Frac-N PLL feedback divider range (see Table 18).

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Bottom part of [Table 19](#) below shows implementation of this step for the 622.08 MHz output frequency example. The combination satisfying above conditions is highlighted in **blue**.

Table 19. Frac-N PLL Feedback Divider and Forward Divider Combination Calculation for Output Frequency = 622.08 MHz

| M D = 2 Within 2 to 8191 | N Within 13.08511 to 15.96875 |
|--------------------------------|----------------------------------|
| 2 | 13.23574 |
| 3 | 19.85362 |
| 4 | 26.47149 |
| 5 | 33.08936 |
| 6 | 39.70723 |
| M D = 1 3, 5 or 7 | N Within 13.08511 to 15.96875 |
| 3 | 9.926808511 |
| 5 | 16.54468085 |
| 7 | 23.16255319 |

Step 3: Select final dividers combination

The criterion for the final dividers combination selection from calculated in steps 1 and 2 is the lowest N value. If one of the steps does not have a valid combination, the one from the other step is selected as final. If there are no valid combinations for both steps, the frequency is out of the supported range.

For the 622.08 MHz example the lowest N value is for forward divider value 2 and D = 2. Step 2 calculation do not have N values within supported range.

Step 4: Calculate N and M Dividers Binary Values (N_reg, M_reg)

The selected combination of N and M values should be converted to binary words and then written to the device's control registers. Number conversion, conditioning and write procedure are as follows. The values calculated in the previous steps for 622.08 MHz output frequency will be used for example purposes.

Step 4.1: Convert N value to binary word

32 bits are intended for Frac-N PLL feedback divider value: MSB 5 bits for integer and LSB 27 for fractional parts

- 1) Take the integer part of the N value and convert to binary.

In our example, integer part is dec: 13 and bin: 01101

- 2) Execute bitwise XOR operation on the integer part (01101b) and 01110b mask.

The reason for the 01110b mask is to set the default value when the device is in an un-programmed state and all bit values are 0.

**N_reg[31:27] = 01101b (given integer part)
XOR 01110b (mask) = 00011b (final value)**

- 3) Fractional part of the N value should be multiplied by 2^{27} and then rounded towards nearest integer. Then it should be converted to binary value resulting in a 27-bit binary word. Because the fractional part of N is always positive, no sign bit should be used. In our example,
 $2^{27} * 0.23574 = 31,641,115.451915$. Rounding to the nearest integer gives 31,641,115 and converting to binary:

**N_reg[31:27] =
001111000101100111000011011b (final value)**

Step 4.2: Convert M value to binary word (M_reg)

- 1) M value should be converted to 13-bit binary word. As forward divider is always positive no sign bit should be used.

In this example, the M value is: 2, bin:
000000000010b

- 2) Execute bitwise XOR operation on the M value and 0000000011011b mask.

**M_reg[12:0] = 000000000010b (given M) XOR
0000000011011b = 0000000011001b (final value)**

Step 4.3: Convert D value to binary word (D_reg)

One bit is dedicated for D control and 0b corresponds to D = 2 and 1b corresponds to D = 1. In our example D = 2 so we will use 0b for D control.

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Step 5: Select appropriate Drive Control values

Select appropriate Drive Control values based on [Table 20](#).

Table 20. Driver Control settings

| Output Driver | Output Frequency (MHz) | Drive Control Reg [5:0] |
|---------------|------------------------|-------------------------|
| LVPECL | 340.000001 to 725 | 101110b |
| LVDS | 340.000001 to 725 | 000000b |
| HCSL | 340.000001 to 500 MHz | 000000b |

In the example, **Drive Control Reg[5:0]: = 101110b**

Step 6: Write N_reg, M_reg, D_reg and driver settings binary values to the device

Write registers to the device in the following sequence

- 1) Address 0x03
 0x03[15:11] = N_reg[31:27] (integer part)
 0x03[10:0] = N_reg[26:16] (fractional part, MSW)
- 2) Address 0x04
 0x04[15:0] = N_reg[15:0] (fractional part, LSW)
- 3) Address 0x06
 0x06[15:2] = Don't care bits
 0x06[3] = D_reg[0]
 0x06[2:0] = Driver Control Reg[2:0]
- 4) Address 0x05
 0x05[15:3] = M_reg[12:0]
 0x05[2:0] = Driver Control Reg[5:3]

After the forward divider value 0x05 is written, the outputs will be disabled until the PLL locks to the new frequency and is stable. When the PLL is stable, the clock output will be re-enabled. [Figure 26](#) and [Figure 27](#) show the write sequence, output disable and programming time for I²C and SPI interfaces.

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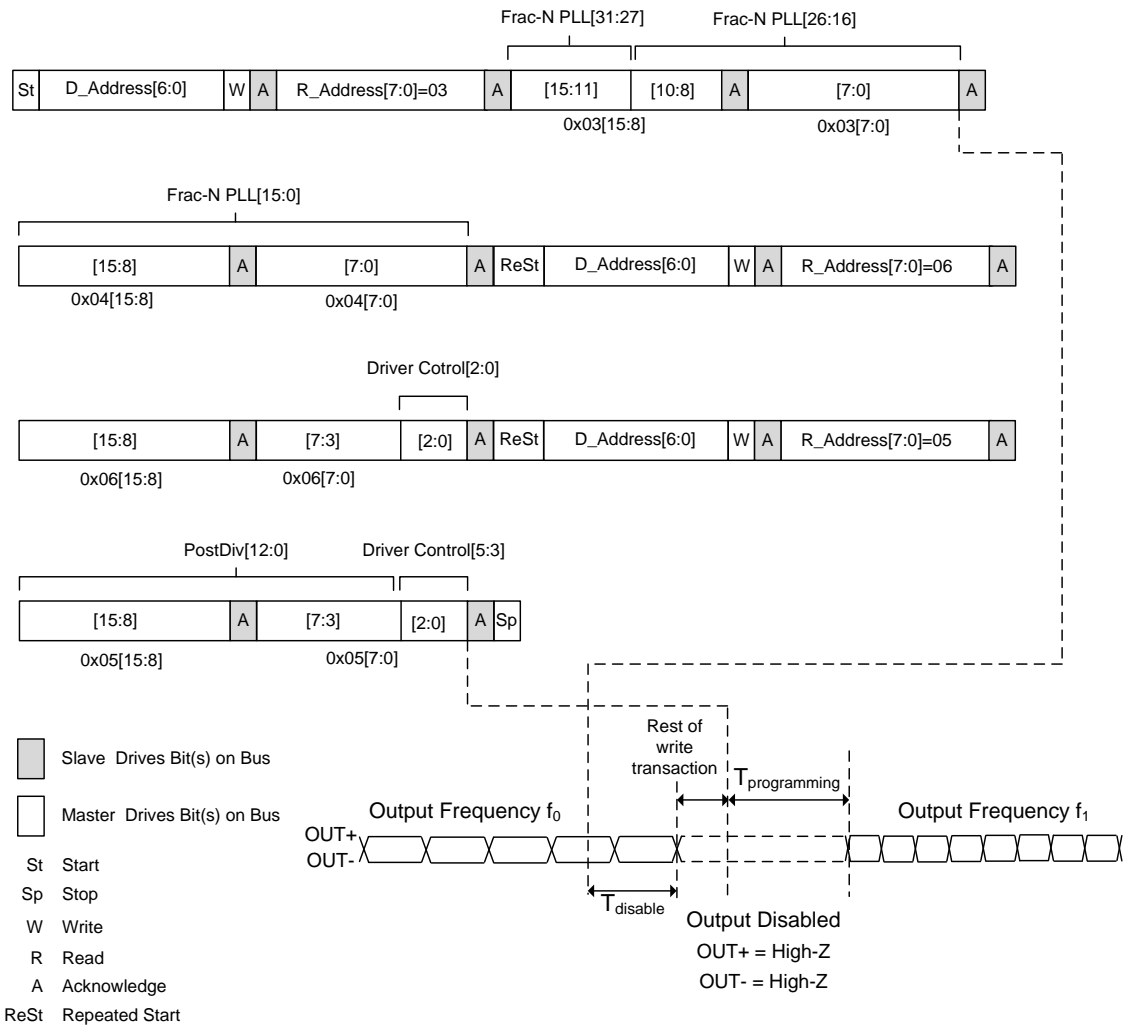


Figure 26. Changing the Default Start-up Output Frequency Using Auto Address Incrementing (I²C)

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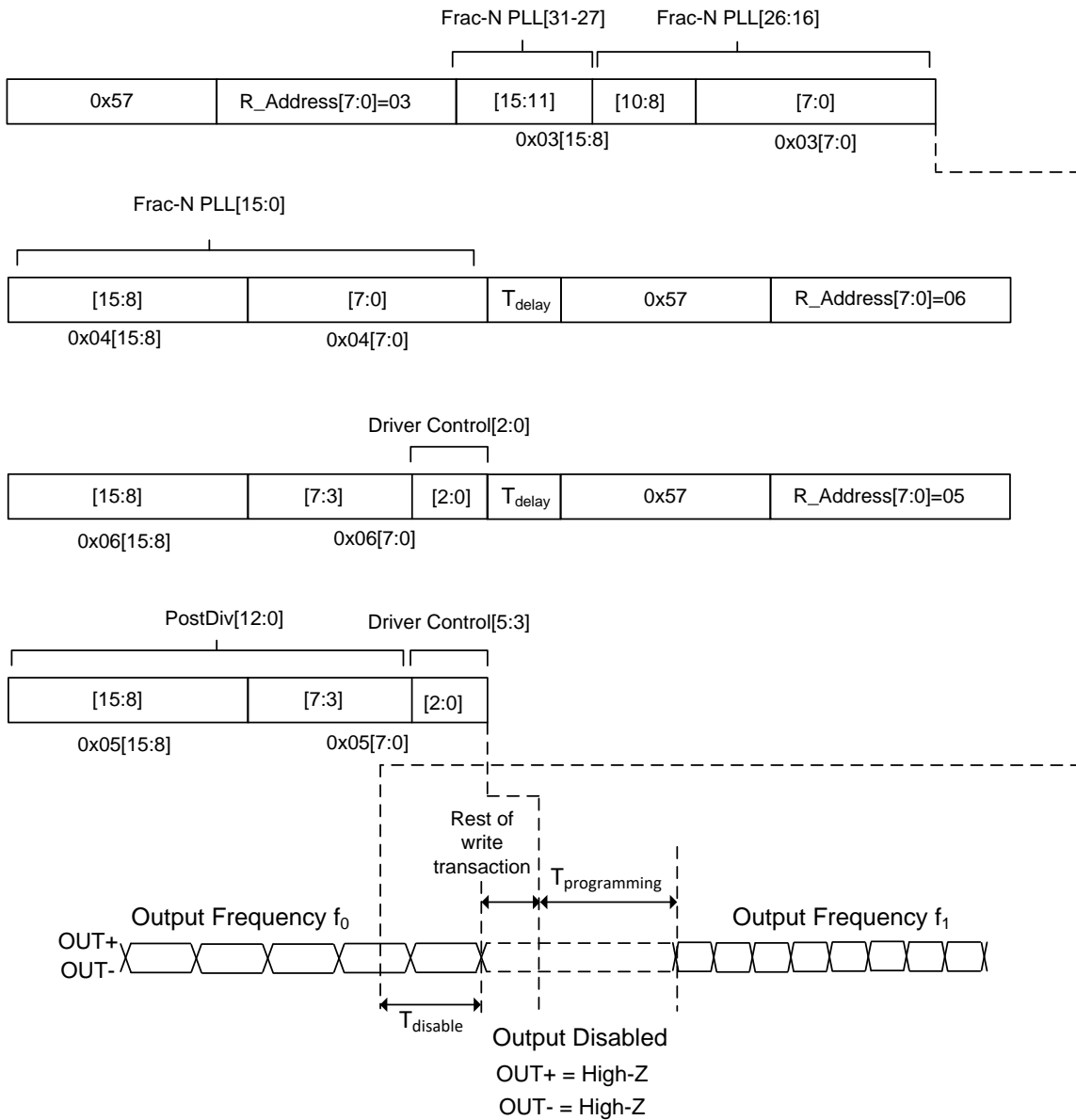


Figure 27. Changing the Default Start-up Output Frequency Using Auto Address Incrementing (SPI)

Table 21. Output Disable and Enable Times when Changing the Output Frequency

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|------------------------------------|-----------------------------|------|------|------|------|-----------------|
| Delay between transactions | T _{delay} | 125 | – | – | µs | SPI only |
| Output Disable Time | T _{disable} | – | 1.9 | 2.3 | µs | At 85°C ambient |
| Settling Time for Frequency Change | T _{re-programming} | – | 414 | 421 | µs | At 85°C ambient |

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8.2. DCO Functional Description

The DCO feature allows users to steer (pull) output frequency by up to ± 3200 ppm with 5 to 94 ppt resolution through the I²C or SPI digital interface.

There are several advantages of DCO relative to analog voltage control (VCXO)

- Frequency Control Resolution as low as 5 ppt. This high resolution minimizes accumulated time error in synchronization applications.
- Lower system cost – A VCXO may need a Digital to Analog Converter (DAC) to drive the control voltage input. In a DCO, the frequency control is achieved digitally by register writes to the control registers via I²C, thereby eliminating the need for a DAC.
- Better Noise Immunity – The analog signal used to drive the voltage control pin of a VCXO can be sensitive to noise and the trace over which the signal is routed can be susceptible to noise coupling from the system. The DCO does not suffer from analog noise coupling since the frequency control is performed digitally through I²C.
- No Frequency Pull non-linearity. The frequency pulling is achieved via fractional feedback divider of the PLL, eliminating any pull non-linearity concern which is typical of quartz based VCXOs. This improves dynamic performance in closed loop operations.
- Programmable Wide Pull Range – The DCO pulling mechanism is via the fractional feedback divider and is therefore not constrained by resonator pullability as in quartz based solutions. The SiT3522 offers 16 frequency pull range options from ± 6.25 ppm to ± 3200 ppm, thereby giving system designers great flexibility.

In the DCO mode, the device powers up at the nominal operating frequency and pull range specified by the ordering code. After power-up both the pull range and output frequency can be controlled via I²C/SPI writes to the respective control registers. The maximum output frequency change is constrained by the pull range limits.

The pull range is specified by the value loaded in the digital pull range control register. The 16 pull range choices are specified in the control register and range from ± 6.25 ppm to ± 3200 ppm.

Table 22 below shows the frequency resolution vs. pull range programmed value.

Table 22. Frequency Resolution vs. Pull Range

| Programmed Pull Range | Frequency Precision |
|-----------------------|-----------------------|
| ± 25 ppm | 5×10^{-12} |
| ± 50 ppm | 5×10^{-12} |
| ± 80 ppm | 5×10^{-12} |
| ± 100 ppm | 5×10^{-12} |
| ± 125 ppm | 5×10^{-12} |
| ± 150 ppm | 5×10^{-12} |
| ± 200 ppm | 5×10^{-12} |
| ± 400 ppm | 1×10^{-11} |
| ± 600 ppm | 1.4×10^{-11} |
| ± 800 ppm | 2.1×10^{-11} |
| ± 1200 ppm | 3.2×10^{-11} |
| ± 1600 ppm | 4.7×10^{-11} |
| ± 3200 ppm | 9.4×10^{-11} |

The ppm frequency offset is specified by the 26-bit DCO Frequency control register in two's complement format as described in the I²C/SPI Register Descriptions. The power up default value is 000000000000000000000000b which sets the output frequency at its nominal value (0ppm). To change the output frequency, a frequency control word is written to 0x00[15:0] (Least Significant Word) and 0x01[9:0] (Most Significant Word). The LSW value should be written first followed by the MSW value; the frequency change is initiated after the MSW value is written.

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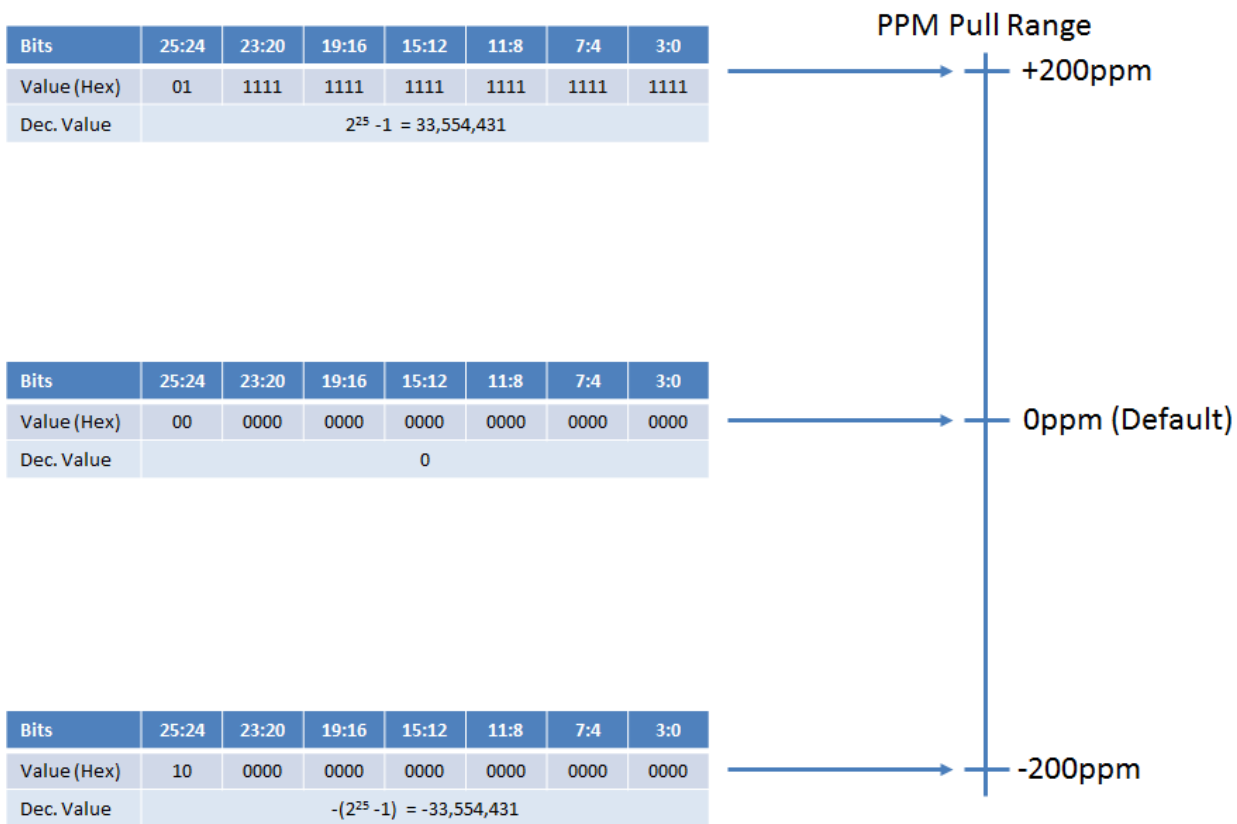


Figure 28. Pull range and Frequency Control Word

Figure 28 shows how the two’s complement signed value of the frequency control word sets the output frequency within the ppm pull range set by 0x02[3:0]. This example shows use of ±200 ppm pull range. Therefore, to set the desired output frequency, one just needs to calculate the fraction of full scale value ppm, convert to two’s complement binary and then write the values to the frequency control registers.

The following formula generates the control word value:

$$\text{Control word Value} = \text{RND}((2^{25}-1) * \text{ppm shift from nominal/pull range})$$

where RND is the rounding function which rounds the number to the nearest whole number.

Two examples follow, assuming the ±200 ppm pull range.

Example 1:

Default start-up output frequency = 156.25 MHz
 Desired output frequency = 156.2640625 MHz (+90 ppm)

$2^{25}-1$ corresponds to +200 ppm, and the fractional value required for +90 ppm can be calculated as follows.
 $90 \text{ ppm}/200 \text{ ppm} * (2^{25}-1) = 15,099,493.95$

Rounding to the nearest whole number yields 15,099,494 and converting to two complement gives a binary value of 111001100110011001100110 and E66666 in hex.

Example 2:

Default start-up output frequency = 122.88 MHz
 Desired output frequency = 122.873856 MHz (-50 ppm)

Following formula shown above,

$$(-50 \text{ ppm}/200 \text{ ppm}) * (2^{25}-1) = -8,388,607.75$$

Rounding to the nearest whole number results in -8,388,608.

Converting to two’s complement binary results in 111000000000000000000000 and 380000 in hex.

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To Summarize, the procedure for calculating the frequency control word associated with a given ppm offset is as follows:

- 1) Calculate the fraction of the half pull range needed. For example, if the total pull range is set for ± 100 ppm and a +20 ppm shift from the nominal frequency is needed, this fraction is $20 \text{ ppm}/100 \text{ ppm} = 0.2$
- 2) Multiply this fraction by the full half scale word value, $2^{25}-1 = 33,554,431$, round to the nearest whole number and convert the result to two's complement binary. Following the +20 ppm example, this value is $0.2 * 33,554,431 = 6,710,886.2$ and rounded to 6,710,886.
- 3) Write the two's complement binary value starting with the Least Significant Word (LSW) 0x00[16:0], followed by the Most Significant Word (MSW), 0x01[9:0]. If the user desires that the output remains enabled while changing the frequency, a 1 must also be written to the OE control bit 0x01[10] if the device has software OE Control Enabled.

It is important to note that the maximum DCO Frequency Control update rate is 38 kHz regardless of I²C/SPI bus speed.

8.3. Pull Range, Absolute Pull Range

Pull range (PR) is the amount of frequency deviation that will result from changing the control voltage over its maximum range under nominal conditions.

Absolute pull range (APR) is the guaranteed controllable frequency range over all environmental and aging conditions. Effectively, it is the amount of pull range remaining after taking into account frequency stability tolerances over variables such as temperature, power supply voltage, and aging, i.e.:

$$APR = PR - F_{stability} - F_{aging}$$

where $F_{stability}$ is the device frequency stability due to initial tolerance and variations on temperature, power supply, and load.

Table 23 below shows the pull range and corresponding APR values for each of the frequency vs. temperature ordering options.

Table 23. DCO Pull Range, APR Options

| Pull Range Ordering Code | Programmed Pull Range ppm | APR ppm ± 10 ppm option | APR ppm ± 20 ppm option | APR ppm ± 25 ppm option | APR ppm ± 50 ppm option |
|--------------------------|---------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|
| M | ± 25 | ± 10 | – | – | – |
| B | ± 50 | ± 35 | ± 25 | ± 20 | – |
| C | ± 80 | ± 65 | ± 55 | ± 50 | ± 25 |
| E | ± 100 | ± 85 | ± 75 | ± 70 | ± 45 |
| G | ± 125 | ± 110 | ± 100 | ± 95 | ± 70 |
| H | ± 200 | ± 185 | ± 175 | ± 170 | ± 145 |
| X | ± 400 | ± 385 | ± 385 | ± 380 | ± 345 |
| Y | ± 800 | ± 785 | ± 785 | ± 780 | ± 745 |
| Z | ± 1600 | ± 1585 | ± 1585 | ± 1580 | ± 1545 |
| U | ± 3200 | ± 3185 | ± 3185 | ± 3180 | ± 3145 |

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Figure 29 below shows the I²C sequence for writing the 4-byte control word using auto address incrementing. It is important to note that if the I²C function is under software control, the software OE control bit 0x01[10] should be “1” during the write sequence to avoid disabling the output.

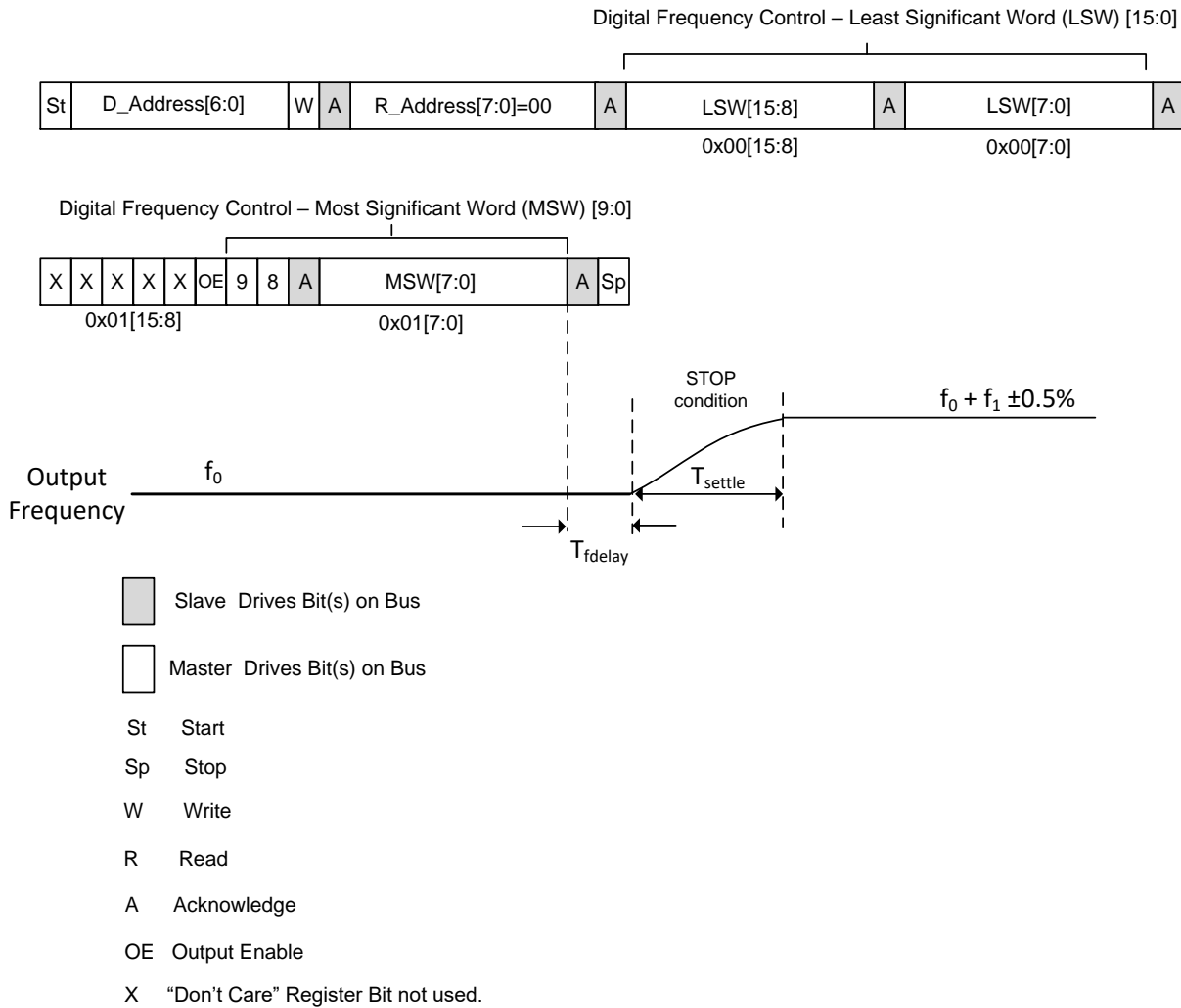


Figure 29. Writing the Frequency Control Word

Table 24. DCO Delay and Settling Time

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|-------------------------|---------------------|------|------|------|------|---|
| Frequency Change Delay | T _{fdelay} | – | 103 | 140 | μs | Time from end of 0x01 reg MSW to start of frequency pull, as shown in Figure 29 |
| Frequency Settling Time | T _{settle} | – | 16.5 | 20 | μs | Time to settle to ±0.5% of frequency offset, as shown in Figure 29 |

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8.4. Software OE Functional Description

Output driver can be enabled or disabled through control registers 0x01[10] (corresponding part number option should be selected to enable this function, please refer to the OE Pin Control option in [Ordering Information](#) section). To enable the output driver, this register should be set to 1, to disable – to 0.

Important note: By default (at startup) output is disabled in this mode and should be enabled by corresponding write operation after start-up.

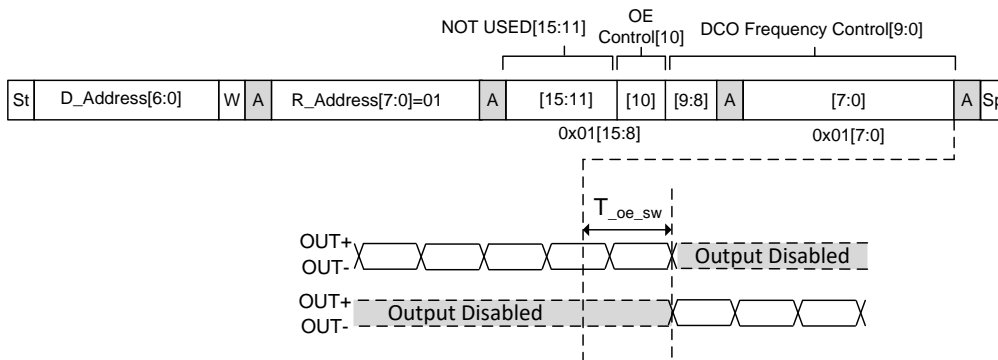


Figure 30. Enable/Disable software OE (I²C)

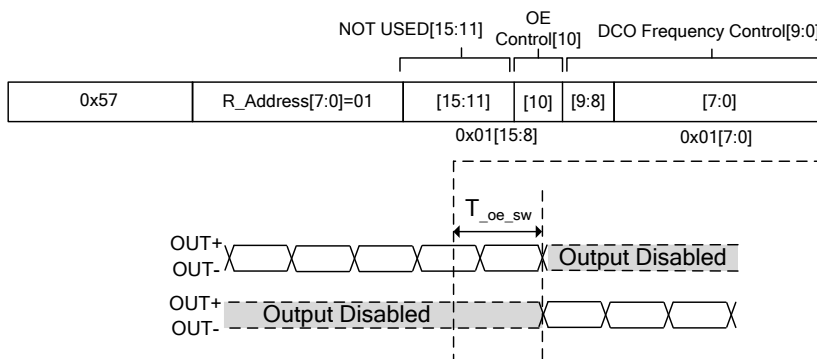


Figure 31. Enable/Disable software OE (I²C)

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9 I²C/SPI Control Registers

The any-frequency, DCO software OE and drive strength control features enable control of frequency pull range, frequency pull value, Output Enable and Drive strength setting via I²C/SPI writes to the control registers.

Table 25 below shows the register map summary and the detailed register descriptions follow.

Table 25. Register Map Summary

| Address | Bits | Access | Description |
|---------|---------|--------|---|
| 0x00 | [15:0] | RW | DCO FREQUENCY CONTROL LEAST SIGNIFICANT WORD (LSW) |
| 0x01 | [15:11] | R | NOT USED |
| | [10] | RW | OE CONTROL. This bit is only active if the output enable function is under software control. If the device is configured for hardware control using an OE pin, writing to this bit has no effect. Selection of Pin or Software OE Control is an ordering option shown in Ordering Information Table . |
| | [9:0] | RW | DCO FREQUENCY CONTROL MOST SIGNIFICANT WORD (MSW) |
| 0x02 | [15:4] | R | NOT USED |
| | [3:0] | RW | DCO PULL RANGE CONTROL |
| 0x03 | [15:11] | RW | FRAC-N PLL FEEDBACK DIVIDER INTEGER VALUE |
| | [10:0] | RW | FRAC-N PLL FEEDBACK DIVIDER FRACTIONAL VALUE, MOST SIGNIFICANT WORD (MSW) |
| 0x04 | [15:0] | RW | FRAC-N PLL FEEDBACK DIVIDER FRACTIONAL VALUE, LEAST SIGNIFICANT WORD (LSW) |
| 0x05 | [15:3] | RW | FORWARD DIVIDER |
| | [2:0] | RW | DRIVER CONTROL |
| 0x06 | [15:2] | R | NOT USED |
| | 3 | RW | DRIVER DIVIDER VALUE |
| | [2:0] | RW | DRIVER CONTROL |

Register Descriptions

9.1. Register Address: 0x00. DCO Frequency Control Least Significant Word (LSW)

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Access | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Name | DCO FREQUENCY CONTROL LEAST SIGNIFICANT WORD (LSW)[15:0] | | | | | | | | | | | | | | | |

| Bits | Name | Access | Description |
|------|--|--------|---|
| 15:0 | DCO FREQUENCY CONTROL LEAST SIGNIFICANT WORD | RW | <p>Bits [15:0] are the lower 16 bits of the 26 bit FrequencyControlWord and are the Least Significant Word (LSW). The upper 10 bits are in register 0x01[9:0] and are the most significant Frequency Control Word (MSW). The lower 16 bits together with upper 10 bits specify a 26-bit frequency control word.</p> <p>This power up default values of all 26 bits are 0 which sets the output frequency at its nominal value. After powerup, the system can write to these two registers to pull the frequency across the pull range. The register values are 2's complement to support positive and negative control values. The LSW value should be written before the MSW value because the frequency change is initiated when the new values are loaded into the MSW. More details and examples are discussed in the next section.</p> |

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9.2. Register Address: 0x01. OE Control, DCO Frequency Control Most Significant Word (MSW)

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----------|----|----|----|----|----|--------------------------------|----|----|----|----|----|----|----|----|----|
| Access | R | R | R | R | R | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Name | NOT USED | | | | | OE | DCO FREQUENCY CONTROL[9:0] MSW | | | | | | | | | |

| Bits | Name | Access | Description |
|-------|---|--------|--|
| 15:11 | NOT USED | R | Bits [15:10] are read only and return all 0's when read. Writing to these bits have no effect. |
| 10 | OE Control | RW | Output Enable Software Control. Allows the user to enable and disable the output driver via I ² C. 0 = Output Disabled (Default) 1 = Output Enabled This bit is only active if the output enable function is under software control. If the device is configured for hardware control using an OE pin, writing to this bit has no effect. |
| 9:0 | DCO FREQUENCY CONTROL MOST SIGNIFICANT WORD (MSW) | RW | Bits [9:0] are the upper 10 bits of the 26 bit Frequency Control Word and are the Most Significant Word (MSW). The lower 16 bits are in register 0x00[15:0] and are the least significant Frequency Control Word (MSW). These lower 16 bits together with upper 10 bits specify a 26-bit frequency control word. This power up default values of all 26 bits are 0 which sets the output frequency at its nominal value. After powerup, the system can write to these two registers to pull the frequency across the pull range. The register values are 2's complement to support positive and negative control values. The LSW value should be written before the MSW value because the frequency change is initiated when the new values are loaded into the MSW. More details and examples are discussed in the next section. |

9.3. Register Address: 0x02. DCO PULL RANGE CONTROL

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|----|----|----|----|----|---|---|---|---|---|---|------------------------|-------------------|-------------------|-------------------|
| Access | R | R | R | R | R | R | R | R | R | R | R | R | RW | RW | RW | RW |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | X ^[13] | X ^[13] | X ^[13] | X ^[13] |
| Name | NONE | | | | | | | | | | | | DCO PULL RANGE CONTROL | | | |

Note:

13. Default values are factory set but can be over-written after power-up.

| Bits | Name | Access | Description |
|------|-------------------------|--------|--|
| 15:4 | NONE | R | Bits [15:4] are read only and return all 0's when read. Writing to these bits have no effect. |
| 3:0 | DCOs PULL RANGE CONTROL | RW | Sets the digital pull range of the DCO. The table below shows the available pull range values and associated bit settings. The default value is factory programmed. Bit 3210 0000: Not used 0001: Not used 0010: Not Used 0011: ±25 ppm 0100: ±50 ppm 0101: ±80 ppm 0110: ±100 ppm 0111: ±125 ppm 1100: ±150 ppm 1001: ±200 ppm 1010: ±400 ppm 1011: ±600 ppm 1100: ±800 ppm 1101: ±1200 ppm 1110: ±1600 ppm 1111: ±3200 ppm |

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9.4. Register Address: 0x03. Frac-N PLL Feedback Divider Integer Value and Frac-N PLL Feedback Divider Fraction Value MSW

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 6 | 5 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|----|----|----|----|----|---|----|----|----|----|----|----|----|----|----|
| Access | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |
| Default | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x |
| Name | Frac-N PLL Feedback Divider Integer Value | | | | | | Frac-N PLL Feedback Divider Fraction Value, MSW | | | | | | | | | |

| Bits | Name | Access | Description |
|-------|---|--------|--|
| 15:11 | Frac-N PLL Feedback Divider Integer Value | RW | Sets the integer value of the Frac-N PLL feedback divider. The default value is factory programmed to correspond to the desired output frequency (hence the x notation in the default value field) and can be changed by the user after powerup. |
| 10:0 | Frac-N PLL Feedback Divider Fraction Value, MSW | RW | Most Significant Word (MSW) of Frac-N PLL feedback divider fraction value. The MSW comprises the upper 11 bits of the 27-bit control word. The default value is factory programmed to correspond to the desired output frequency (hence the x notation in the default value field) and can be changed by the user after powerup. |

9.5. Register Address: 0x04. Frac-N PLL Feedback Divider Fraction Value LSW

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 6 | 5 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Access | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |
| Default | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x |
| Name | Frac-N PLL Feedback Divider Fraction Value, LSW | | | | | | | | | | | | | | | |

| Bits | Name | Access | Description |
|------|---|--------|--|
| 15:0 | Frac-N PLL Feedback Divider Fraction Value, LSW | RW | Sets the Least Significant Word of the Frac-N PLL feedback divider fraction value. The default value is factory programmed to correspond to the desired output frequency (hence the x notation in the default value field) and can be changed by the user after powerup. |

9.6. Register Address: 0x05. Forward Divider, Driver Control

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----------------|----|----|
| Access | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |
| Default | x | x | x | x | x | x | x | x | x | x | x | x | x | 0 | 0 | 0 |
| Name | Forward Divider | | | | | | | | | | | | | Driver Control | | |

| Bits | Name | Access | Description | |
|------|-----------------------|--------|---|-----------------------|
| 15:3 | Forward Divider | RW | Forward Divider Value. The default value is factory programmed to correspond to the desired output frequency (hence the x notation in the default value field) and can be changed by the user after powerup. The Forward Divider Value Range is [2:8191]. | |
| 2:0 | Driver Control. | RW | LVDS or HCSL driver | |
| | | | Bit Value | Frequency range |
| | | | 001 | 1 to 250 MHz |
| | | | 000 | 250.000001 to 340 MHz |
| | | | LVPECL driver | |
| | | | Bit Value | Frequency range |
| 110 | 1 to 250 MHz | | | |
| 101 | 250.000001 to 340 MHz | | | |

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9.7. Register Address: 0x06. Driver Divider, Driver Control

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----------|----|----|----|----|----|---|---|---|---|---|---|----------------|----------------|----|----|
| Access | R | R | R | R | R | R | R | R | R | R | R | R | RW | RW | RW | RW |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Name | NOT USED | | | | | | | | | | | | Driver Divider | Driver Control | | |

| Bits | Name | Access | Description | |
|------|----------------|--------|---|-----------------|
| 15:4 | NOT USED | R | Bits [15:4] are read only and return all 0's when read. Writing to these bits have no effect. | |
| 3 | Driver Divider | RW | Driver divider value. | |
| | | | Bit Value | mDriver |
| | | | 0 | 2 |
| 1 | 1 (bypass) | | | |
| 2:0 | Driver Control | RW | LVDS or HCSL driver | |
| | | | Bit Value | Frequency range |
| | | | 000 | 1 to 340 MHz |
| | | | LVPECL driver | |
| 110 | 1 to 340 MHz | | | |

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10 I²C Operation

10.1. I²C protocol

Data valid

The SDA line must be stable during the high period of the SCLK. SDA transitions are allowed only during SCLK low level for data communication. Only one transition is allowed during low SCLK pulse to communicate one bit of data. [Figure 32](#) shows the detailed timing diagram.

START and STOP conditions

The idle I²C bus state occurs when both SCLK and SDA are not being driven by any master and are therefore in a logic HI state due to the pull up resistors. Every transaction begins with a START (S) signal and ends with a STOP (P) signal. A START condition is defined by a high to low transition on the SDA while SCLK is high. A STOP condition is defined by a low to high transition on the SDA while SCLK is high. START and STOP conditions are always generated by master. This slave module also supports repeated START (Sr) condition which is same as START condition instead of STOP condition (Blue color line shows repeated START in [Figure 33](#)).

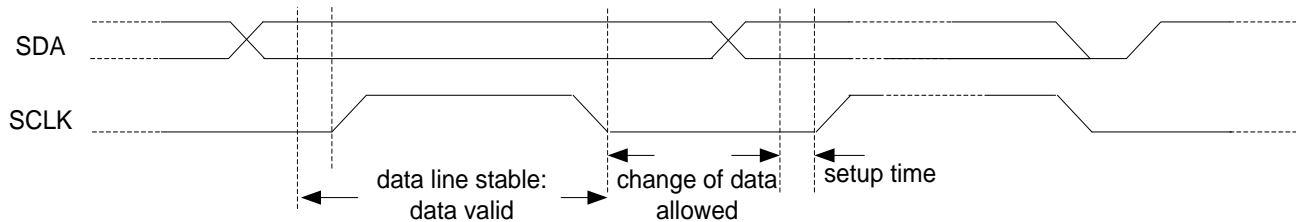


Figure 32. Data and clock timing relation in I²C bus

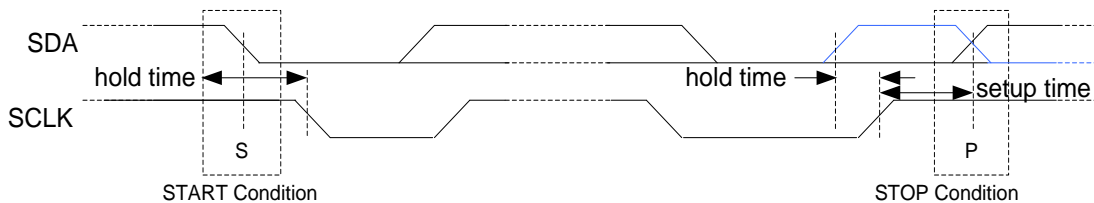


Figure 33. START and STOP (or repeated START) condition

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Data Transfer Format

Every data byte is eight bits long. The number of bytes that can be transmitted per transfer is unrestricted. Data is transferred with the MSB (Most Significant Bit) first. The detailed data transfer format is shown in [Figure 34](#) below.

The acknowledge bit must occur after every byte transfer and it allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. The acknowledge signal is defined as follows: the transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line low and it remains stable low during the high period of this clock pulse. Setup and hold times must also be taken into account. When SDA remains high during this ninth clock pulse, this is defined as the Not-Acknowledge signal (NACK). The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer. The only condition that leads to the generation of NACK from the SiT3522 is when the transmitted address does not match the slave address. When the master is reading data from SiT3522, the SiT3522 expects the ACK from the master at the end of received data, so that the slave releases the SDA line and the master can generate the STOP or repeated START. If there is NACK signal at the end of data, then the SiT3522 tries to send the next data. If the first bit of next data is "0", then the SiT3522 holds the SDA line to "0", thereby blocking the master from generating a STOP/(re)START signal.

Write/Read sequence

This I²C slave module supports 7-bit device addressing format. The 8th bit is a read/write bit and "1" indicates a read transaction and a "0" indicates a write transaction. The register addresses are 8-bits long with an address range of 0 to 255 (00h to FFh). Auto address incrementing is supported which allows data to be transferred to contiguous addresses without the need to write each address beyond the first address. Since the maximum register address value is 255, the address will roll from 255 to back to 0 when auto address incrementing is used. Obviously, auto address incrementing should only be used for writing to contiguous addresses. The data format is 16-bit (two bytes) with the most significant byte being transferred first. For a read operation, the starting register address must be written first. If that is omitted, reading will start from the last address in the auto-increment counter of the device, which has a startup default of 0x00.

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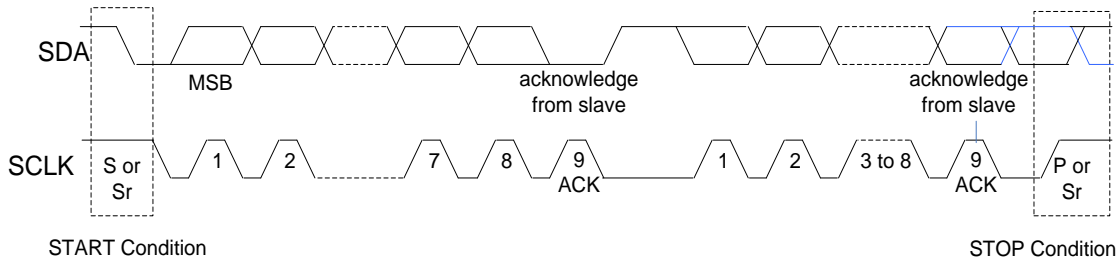


Figure 34. Data Transfer Format

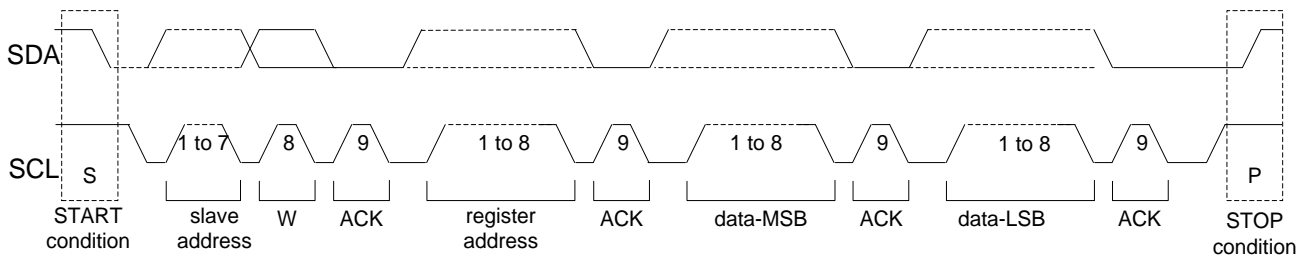


Figure 35. Write Sequence

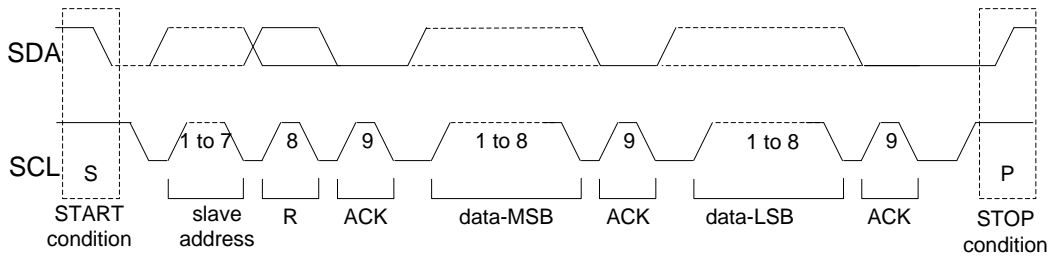


Figure 36. Read Sequence

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10.2. I²C Timing Specification

The below timing diagram and table illustrate the timing relationships for both master and slave.

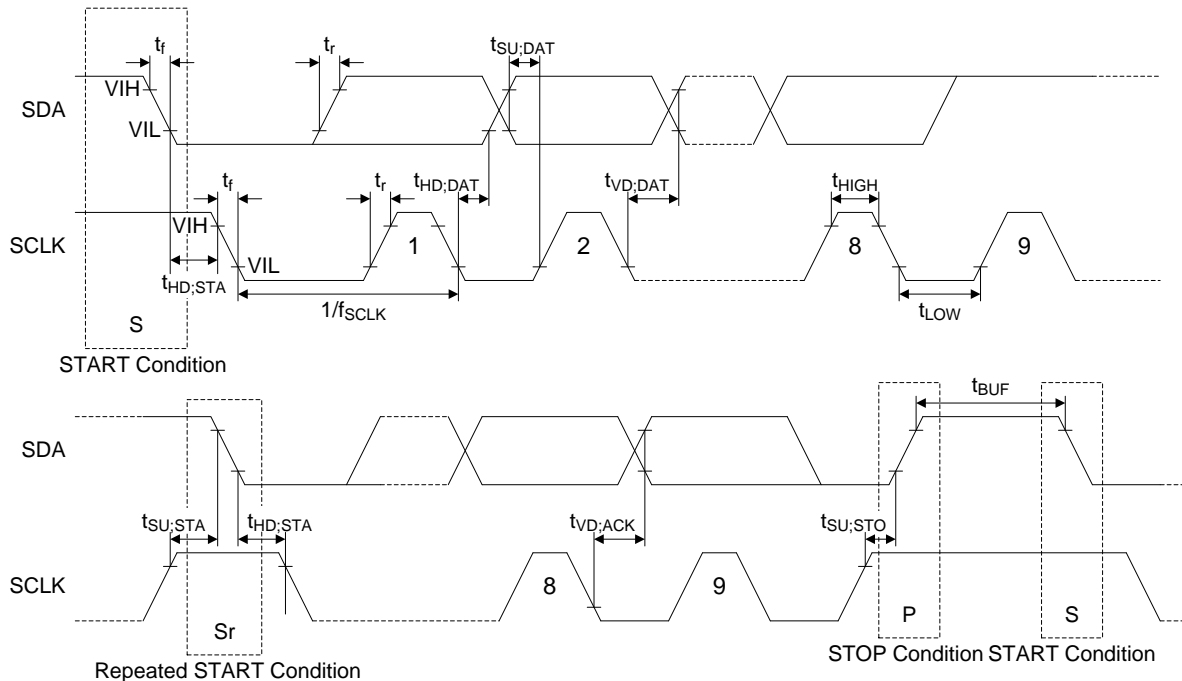


Figure 37. I²C Timing Diagram

Table 26. I²C Timing Requirements

All Min and Max limits are specified over temperature and rated operating voltage with 255 Ohm resistor and 550 pF output load unless otherwise stated. Typical values are at 25°C and nominal supply voltage.

| Parameter | Symbol | Standard mode | | | Fast mode | | | Fast mode plus ^[14] | | | Unit |
|---|---------------------|---------------|------|------|-----------|------|------|--------------------------------|------|------|------|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| SCLK clock frequency | f _{SCLK} | – | – | 100 | – | – | 400 | – | – | 1000 | kHz |
| Low period of SCLK clock | t _{LOW} | 500 | – | – | 500 | – | – | 500 | – | – | ns |
| High period of SCLK clock | t _{HIGH} | 260 | – | – | 260 | – | – | 260 | – | – | ns |
| Rise time of both SCLK and SDA | t _r | – | – | 120 | – | – | 120 | – | – | 120 | ns |
| Fall time of both SCLK and SDA | t _f | 30 | – | 300 | 30 | – | 300 | 30 | – | 120 | ns |
| Hold time for Start condition | t _{HD:STA} | 260 | – | – | 260 | – | – | 260 | – | – | ns |
| Setup time for Start condition | t _{SU:STA} | 260 | – | – | 260 | – | – | 260 | – | – | ns |
| Data setup time | t _{SU:DAT} | 50 | – | – | 50 | – | – | 50 | – | – | ns |
| Data hold time | t _{HD:DAT} | 0 | – | – | 0 | – | – | 0 | – | – | ns |
| Data valid time | t _{VD:DAT} | – | – | 450 | – | – | 450 | – | – | 450 | ns |
| Data valid acknowledge time | t _{VD:ACK} | – | – | 450 | – | – | 450 | – | – | 450 | ns |
| Setup time for stop condition | t _{SU:STO} | 260 | – | – | 260 | – | – | 260 | – | – | ns |
| I ² C bus free time between stop and start | t _{BUF} | 500 | – | – | 500 | – | – | 500 | – | – | ns |

Notes:

14. Fast mode plus is not supported in Extended Industrial temperature range.

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10.3. I²C Device Address Modes

There are two I²C Address modes:

- 1) Factory Programmed Mode. The lower 4 bits of the 7-bit device address are set by ordering code as shown in [Table 27](#) below. There are 16 factory programmed addresses available. In this mode, pins 4 and 5 are NC and pin control of the I²C address is not available.
- 2) A0, A1 Pin Control. This mode allows the user to select between four I²C Device addresses as shown in [Table 28](#).

Table 27. Factory Programmed I²C Address Control

| I ² C Address Ordering Code | Device I ² C Address |
|--|---------------------------------|
| 0 | 1100000 |
| 1 | 1100001 |
| 2 | 1100010 |
| 3 | 1100011 |
| 4 | 1100100 |
| 5 | 1100101 |
| 6 | 1100110 |
| 7 | 1100111 |
| 8 | 1101000 |
| 9 | 1101001 |
| A | 1101010 |
| B | 1101011 |
| C | 1101100 |
| D | 1101101 |
| E | 1101110 |
| F | 1101111 |

[Table 28](#) is only valid for the ordering option which does not use the I²C address pins A0, A1.

Table 28. Pin Selectable I²C Address Control

| A1 Pin 4 | A0 Pin 5 | I ² C Address |
|-------------|-------------|--------------------------|
| 0 | 0 | 1100000 |
| 0 | 1 | 1100010 |
| 1 | 0 | 1101000 |
| 1 | 1 | 1101010 |

[Ordering Information Table](#) is only valid for the ISP-DCXO device option which uses pin control (A0, A1) of the I²C address. This mode corresponds to ordering code "G" in the I²C address section of the ordering code table.

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11 SPI Operation

SPI (Serial Peripheral Interface) is a 4-pin synchronous serial protocol that allows a master device to initiate half-duplex communication with one or more slave devices. The pin functions are as follows:

SCLK: Serial Clock which supports up to 6.35 MHz operating frequency.

MOSI: Master Output Slave Input. This is the data input pin to the SiT3522 and is used by the master to write data to the SiT3522 control registers.

MISO: Master Input Slave Output. This is the data output pin of the SiT3522 and is used by the master to read data from the SiT3522 control registers.

SS: Active Low SPI Chip Select. This pin is used by the master to select the SiT3522 as the active slave device on the SPI bus. When the master drives the SiT3522 pin low, the SiT3522 is selected as the target of a read or write transaction.

The following [Figure 38](#) illustrates the logical connection between one SPI master and 3 SPI slaves. Note that this diagram shows only an example logical connection and is not a detailed schematic intended to show pull-up resistors and other components which may also be required.

There are two allowed states for idle SCLK state, HI and LOW and these states are called clock phase. There are also two modes for clock sampling edge, rising edge and falling edge and these modes are called clock polarity. Since there are two allowed clock phases and two allowed clock polarities, this means there are four total modes of SPI operation as illustrated below in [Figure 39](#).

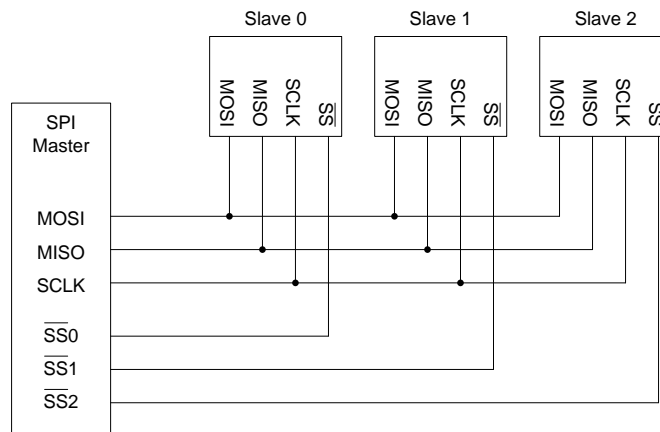


Figure 38. Multi-slave SPI bus connections

| Mode | SCLK Polarity SCLK_POL | SCLK Phase SCLK_PHA |
|--------|---------------------------|------------------------|
| Mode 0 | Low At Start | Rising Edge |
| Mode 1 | Low At Start | Falling Edge |
| Mode 2 | High At Start | Falling Edge |
| Mode 3 | High At Start | Rising Edge |

Figure 39. SPI operation modes

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The SiT3522 can support all four operating modes. By default, modes 0 and 3 are supported, but modes 1 and 2 can be supported in the future.

The serial byte interface format is shown below: 8-bit command (read or write), 8-bit SPI address and 16-bit data.

The serial order is most significant bit (MSB) first. The SPI protocol also supports auto address incrementing which means the address will automatically increment after the first transaction. Auto address incrementing will result in higher data throughput when writing to registers with contiguous addresses. If it is required to write to non-contiguous addresses, a write command and register address must be used for each transaction after the delay (125 us min). Without such delay, the device will consider command and address bytes as a data for the consequent register.

The detail register descriptions are covered in the [I²C/SPI Control Registers](#).

A description of DCO control is in [DCO Functional Description](#) and a description of changing the output center frequency is in [Any-frequency Functional Description](#).

The below [Figure 41](#) shows the timing diagram for modes 0 and 3.

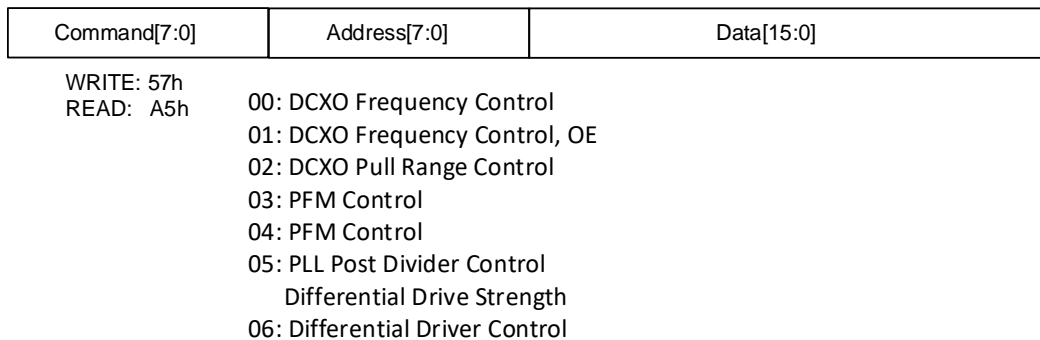


Figure 40. SPI control word format

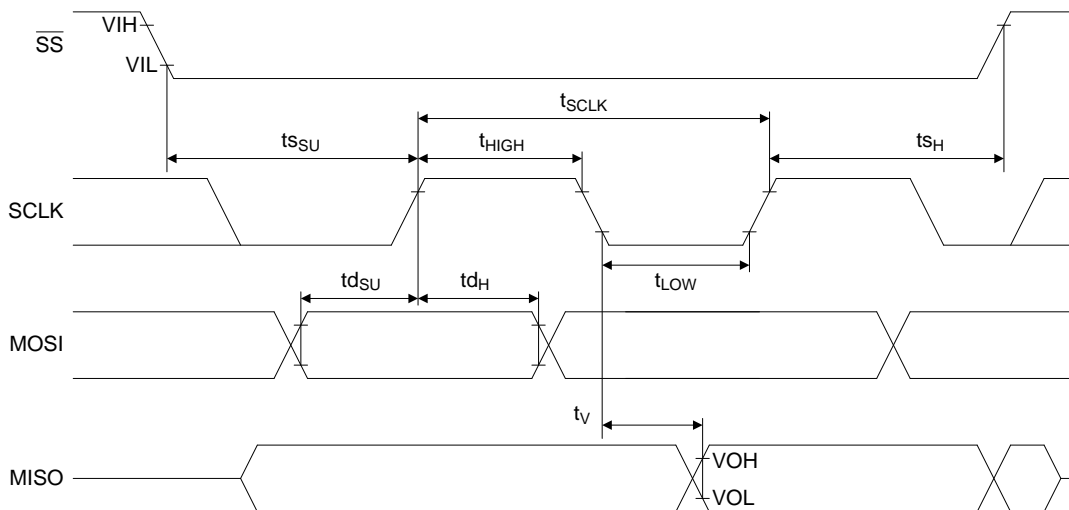


Figure 41. SPI Timing Diagram (Mode 0/3)

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Table 29. SPI Timing Requirements^[15]

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|------------|----------------------|--------------|------|------|
| Setup time for MOSI to SCLK Rising Edge | t_{dsu} | 28 | – | – | ns |
| Hold time for MOSI to SCLK Rising edge | t_{dH} | 1 | – | – | ns |
| Time from active edge of SCLK clock to valid MISO data available at pin | t_v | – | – | 30 | ns |
| Period of SCLK | t_{sCLK} | – | – | 200 | ns |
| High Width of SCLK | t_{HIGH} | – | $t_{sCLK}/2$ | – | ns |
| Low Width of SCLK | t_{LOW} | – | $t_{sCLK}/2$ | – | ns |
| Setup time for SSB falling edge to SCLK rising edge | t_{ssu} | $1.5 \cdot t_{sCLK}$ | – | – | ns |
| Hold time from SSB rising edge to SCLK rising edge | t_{sH} | $1.5 \cdot t_{sCLK}$ | – | – | ns |

Notes:

15. SPI is not supported in Extended Industrial temperature range.

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Schematic Examples

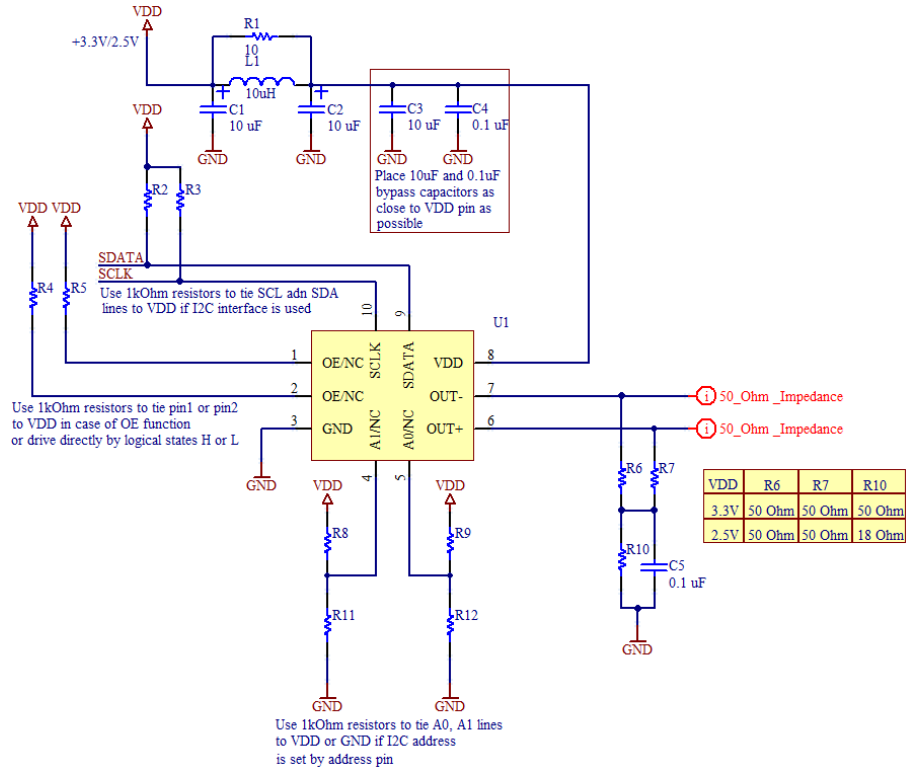


Figure 42. Schematic Example (LVPECL, I²C mode)

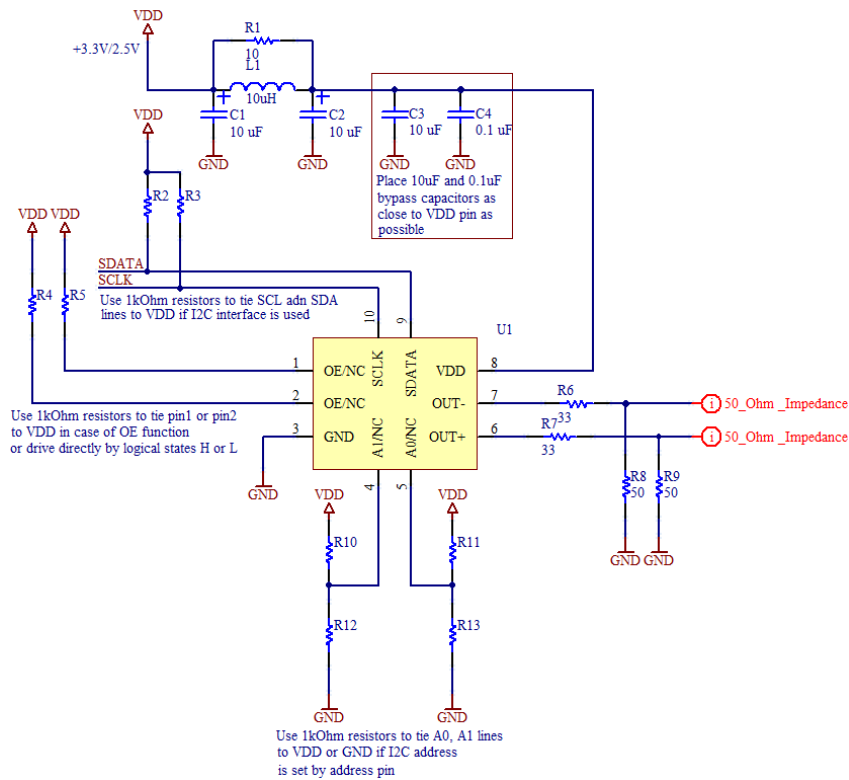


Figure 43. Schematic Example (HCSL, I²C mode)

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Schematic Examples (continued)

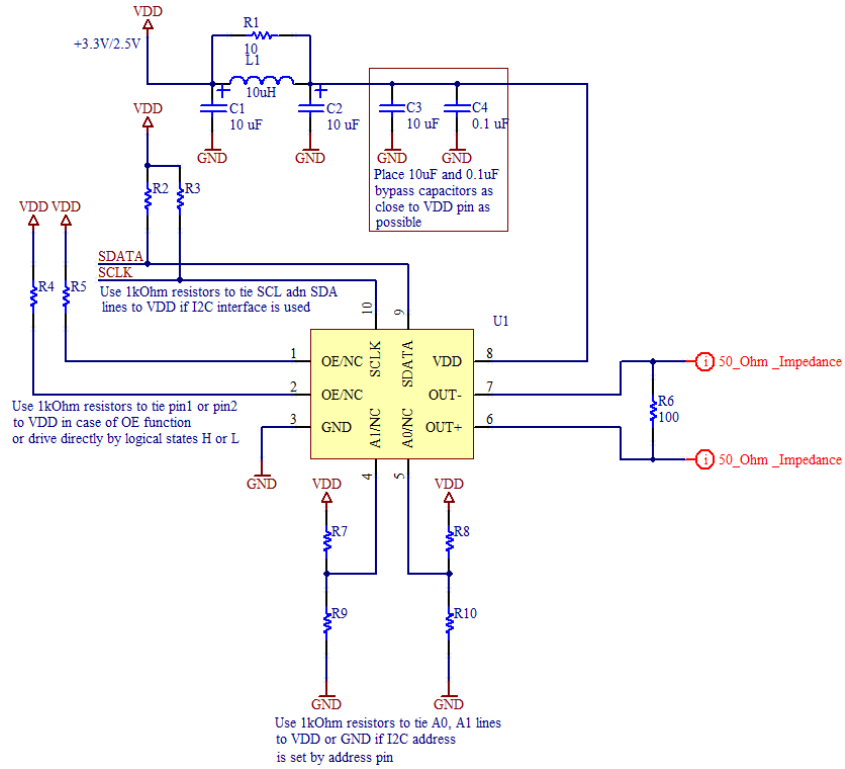


Figure 44. Schematic Example (LVDS, I²C mode)

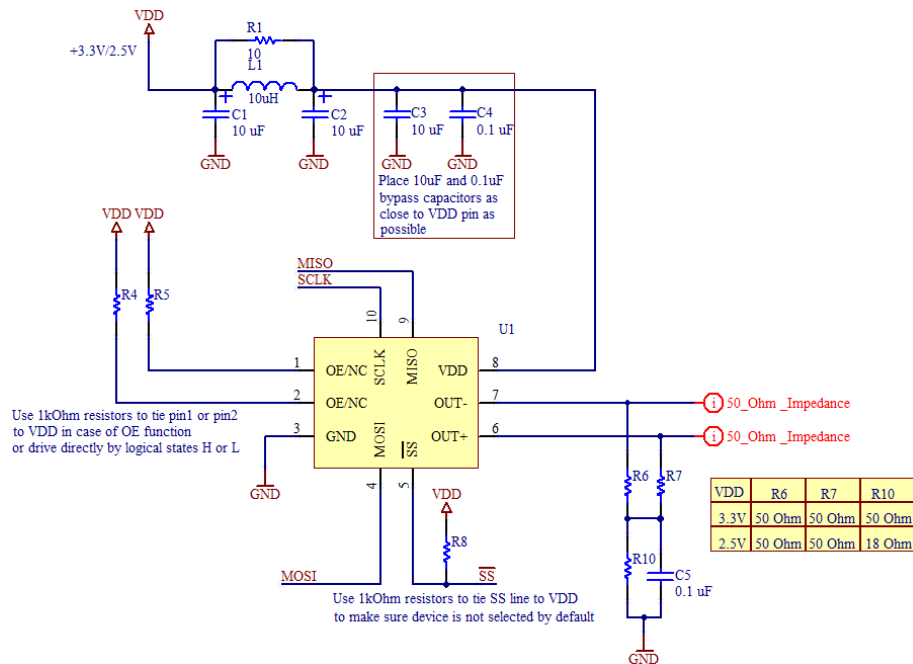


Figure 45. Schematic Example (LVPECL, SPI mode)

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Schematic Examples (continued)

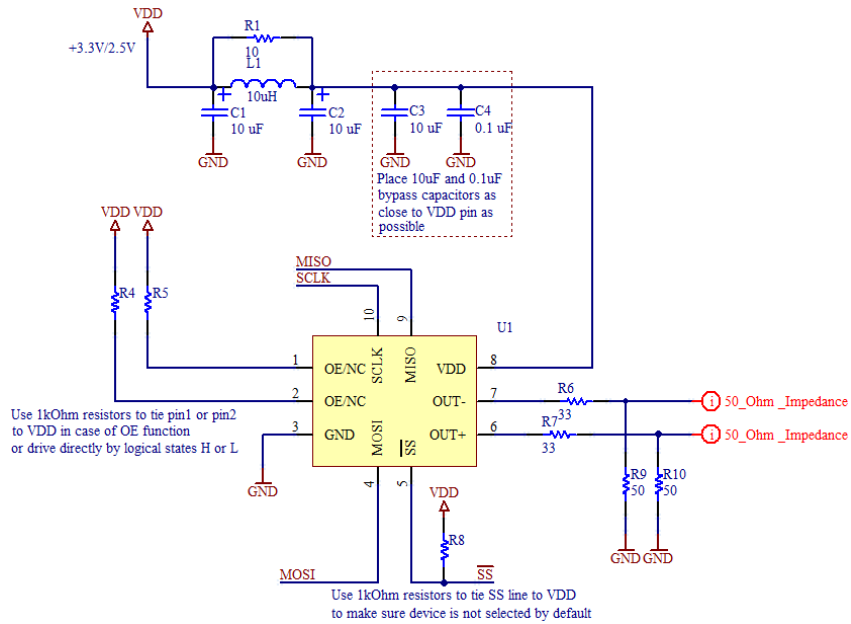


Figure 46. Schematic Example (HCSL, SPI mode)

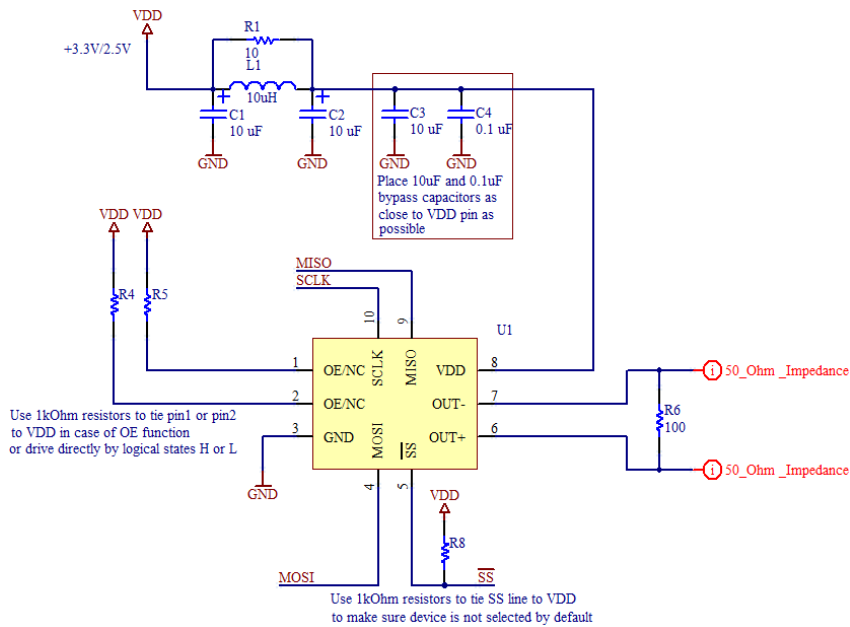


Figure 47. Schematic Example (LVDS, SPI mode)

SiT3522 340 to 725 MHz Elite Platform I2C/SPI Programmable Oscillator



Dimensions and Patterns

| Package Size – Dimensions (Unit: mm) ^[16] | Recommended Land Pattern (Unit: mm) ^[17] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|-----------|-------|-------|-----|-----------------|---|-------|-------|-------|-----------|----|-------|-------|-------|-----------|---|-----------|--|--|---|-----------|--|--|---------|---|-------|-------|-------|---|-------|-------|-------|------------|---|-------|-------|-------|----|-------|-------|-------|-------------|---|-------|-------|-------|----|-----------|--|--|------------|----|-------|-------|-------|---|-----------|--|--|-------------------|-----|-------|--|--|---------------|-----|-------|--|--|------------|-----|-------|--|--|--------------|---|-----------|--|--|---------------|---|-----------|--|--|--------------|----|-----------|--|--|-----------------|--|----------|-------------------------|---------------------|--|------------|--|--|---------------------|--|---------|--------------|---------------------|--|------------|--|
| <p>5.0 x 3.2 x 0.85 mm</p> <div style="float: right; width: 30%;"> <table border="1" style="font-size: 8px; border-collapse: collapse;"> <thead> <tr> <th></th> <th>SYMBOL</th> <th>MIN</th> <th>NOM</th> <th>MAX</th> </tr> </thead> <tbody> <tr> <td>TOTAL THICKNESS</td> <td>A</td> <td>0.800</td> <td>0.850</td> <td>0.900</td> </tr> <tr> <td>STAND OFF</td> <td>A1</td> <td>0.000</td> <td>0.035</td> <td>0.050</td> </tr> <tr> <td rowspan="2">BODY SIZE</td> <td>X</td> <td colspan="3">5.000 BSC</td> </tr> <tr> <td>Y</td> <td colspan="3">3.200 BSC</td> </tr> <tr> <td rowspan="2">EP SIZE</td> <td>X</td> <td>3.100</td> <td>3.200</td> <td>3.300</td> </tr> <tr> <td>Y</td> <td>0.300</td> <td>0.400</td> <td>0.500</td> </tr> <tr> <td rowspan="2">LEAD WIDTH</td> <td>b</td> <td>0.590</td> <td>0.640</td> <td>0.690</td> </tr> <tr> <td>b1</td> <td>0.350</td> <td>0.400</td> <td>0.450</td> </tr> <tr> <td rowspan="2">LEAD LENGTH</td> <td>L</td> <td>0.850</td> <td>0.900</td> <td>0.950</td> </tr> <tr> <td>L1</td> <td colspan="3">1.000 REF</td> </tr> <tr> <td rowspan="2">LEAD PITCH</td> <td>L2</td> <td>0.450</td> <td>0.500</td> <td>0.550</td> </tr> <tr> <td>e</td> <td colspan="3">1.270 BSC</td> </tr> <tr> <td>PACKAGE TOLERANCE</td> <td>aaa</td> <td colspan="3">0.100</td> </tr> <tr> <td>MOLD FLATNESS</td> <td>bbb</td> <td colspan="3">0.100</td> </tr> <tr> <td>COPLANRITY</td> <td>ccc</td> <td colspan="3">0.080</td> </tr> <tr> <td>DIMPLE WIDTH</td> <td>T</td> <td colspan="3">0.300 REF</td> </tr> <tr> <td>DIMPLE LENGTH</td> <td>P</td> <td colspan="3">0.150 REF</td> </tr> <tr> <td>DIMPLE DEPTH</td> <td>A2</td> <td colspan="3">0.100 REF</td> </tr> </tbody> </table> <p>NOTES 1. Dimensioning and tolerancing conform to ASME Y14.5-2009. 2. All dimensions are in millimeters.</p> <table border="1" style="margin-top: 10px; font-size: 8px; border-collapse: collapse; width: 100%;"> <thead> <tr> <th colspan="2" style="text-align: center;">Package Outline</th> </tr> </thead> <tbody> <tr> <td style="width: 50%;">10L PQFV</td> <td>POD-PQFV-010-C05032-040</td> </tr> <tr> <td>5.0 x 3.2 x 0.85 mm</td> <td style="text-align: center;"></td> </tr> <tr> <td>2019/03/13</td> <td></td> </tr> </tbody> </table> </div> <td style="vertical-align: top;"> <table border="1" style="margin-top: 10px; font-size: 8px; border-collapse: collapse; width: 100%;"> <thead> <tr> <th colspan="2" style="text-align: center;">Solder Print Layout</th> </tr> </thead> <tbody> <tr> <td style="width: 50%;">10L QFN</td> <td>SPL-001-RevA</td> </tr> <tr> <td>5.0 x 3.2 x 0.85 mm</td> <td style="text-align: center;"></td> </tr> <tr> <td>2017/11/29</td> <td></td> </tr> </tbody> </table> </td> | | SYMBOL | MIN | NOM | MAX | TOTAL THICKNESS | A | 0.800 | 0.850 | 0.900 | STAND OFF | A1 | 0.000 | 0.035 | 0.050 | BODY SIZE | X | 5.000 BSC | | | Y | 3.200 BSC | | | EP SIZE | X | 3.100 | 3.200 | 3.300 | Y | 0.300 | 0.400 | 0.500 | LEAD WIDTH | b | 0.590 | 0.640 | 0.690 | b1 | 0.350 | 0.400 | 0.450 | LEAD LENGTH | L | 0.850 | 0.900 | 0.950 | L1 | 1.000 REF | | | LEAD PITCH | L2 | 0.450 | 0.500 | 0.550 | e | 1.270 BSC | | | PACKAGE TOLERANCE | aaa | 0.100 | | | MOLD FLATNESS | bbb | 0.100 | | | COPLANRITY | ccc | 0.080 | | | DIMPLE WIDTH | T | 0.300 REF | | | DIMPLE LENGTH | P | 0.150 REF | | | DIMPLE DEPTH | A2 | 0.100 REF | | | Package Outline | | 10L PQFV | POD-PQFV-010-C05032-040 | 5.0 x 3.2 x 0.85 mm | | 2019/03/13 | | <table border="1" style="margin-top: 10px; font-size: 8px; border-collapse: collapse; width: 100%;"> <thead> <tr> <th colspan="2" style="text-align: center;">Solder Print Layout</th> </tr> </thead> <tbody> <tr> <td style="width: 50%;">10L QFN</td> <td>SPL-001-RevA</td> </tr> <tr> <td>5.0 x 3.2 x 0.85 mm</td> <td style="text-align: center;"></td> </tr> <tr> <td>2017/11/29</td> <td></td> </tr> </tbody> </table> | Solder Print Layout | | 10L QFN | SPL-001-RevA | 5.0 x 3.2 x 0.85 mm | | 2017/11/29 | |
| | SYMBOL | MIN | NOM | MAX | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| TOTAL THICKNESS | A | 0.800 | 0.850 | 0.900 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| STAND OFF | A1 | 0.000 | 0.035 | 0.050 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| BODY SIZE | X | 5.000 BSC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | Y | 3.200 BSC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| EP SIZE | X | 3.100 | 3.200 | 3.300 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | Y | 0.300 | 0.400 | 0.500 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| LEAD WIDTH | b | 0.590 | 0.640 | 0.690 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | b1 | 0.350 | 0.400 | 0.450 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| LEAD LENGTH | L | 0.850 | 0.900 | 0.950 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | L1 | 1.000 REF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| LEAD PITCH | L2 | 0.450 | 0.500 | 0.550 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | e | 1.270 BSC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PACKAGE TOLERANCE | aaa | 0.100 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| MOLD FLATNESS | bbb | 0.100 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| COPLANRITY | ccc | 0.080 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| DIMPLE WIDTH | T | 0.300 REF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| DIMPLE LENGTH | P | 0.150 REF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| DIMPLE DEPTH | A2 | 0.100 REF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Package Outline | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 10L PQFV | POD-PQFV-010-C05032-040 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5.0 x 3.2 x 0.85 mm | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2019/03/13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Solder Print Layout | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 10L QFN | SPL-001-RevA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5.0 x 3.2 x 0.85 mm | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2017/11/29 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Notes:

- 16. Top Marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of “Y” will depend on the assembly location of the device.
- 17. The center pad has no electrical function. Soldering down the center pad to the GND is recommended for best thermal dissipation, but is optional.

SiT3522 340 to 725 MHz Elite Platform I2C/SPI Programmable Oscillator

Additional Information
Table 30. Additional Information

| Document | Description | Download Link |
|--|--|---|
| ECCN #: EAR99 | Five character designation used on the commerce Control List (CCL) to identify dual use items for export control purposes. | — |
| HTS Classification Code: 8542.39.0000 | A Harmonized Tariff Schedule (HTS) code developed by the World Customs Organization to classify/define internationally traded goods. | — |
| Part number Generator | Tool used to create the part number based on desired features. | https://www.sitime.com/part-number-generator |
| Manufacturing Notes | Tape & Reel dimension, reflow profile and other manufacturing related info | https://www.sitime.com/support/resource-library/manufacturing-notes-sitime-products |
| Qualification Reports | RoHS report, reliability reports, composition reports | http://www.sitime.com/support/quality-and-reliability |
| Performance Reports | Additional performance data such as phase noise, current consumption and jitter for selected frequencies | http://www.sitime.com/support/performance-measurement-report |
| Termination Techniques | AN10029 Termination design recommendations | http://www.sitime.com/support/application-notes |
| Layout Techniques | AN10006 Layout recommendations | http://www.sitime.com/support/application-notes |
| Time Master Web Based Configurator | Tool to establish proper programming | https://www.sitime.com/time-master-web-based-configurator |
| Evaluation Boards | SiT6712EB Evaluation Board User Manual | https://www.sitime.com/support/user-guides |
| Demo Boards | SiT6701DM, SiT6702DM Demo Board User Manual | https://www.sitime.com/support/user-guides |

SiT3522 340 to 725 MHz Elite Platform I2C/SPI Programmable Oscillator


Revision History

Table 31. Revision History

| Revisions | Release Date | Change Summary |
|-----------|--------------|--|
| 0.1 | Mar 3, 2017 | Initial draft |
| 0.2 | Mar 10, 2017 | Added I ² C Timing diagram for ISP Function Modified Block Diagram to include approximate MEMS frequency (47 MHz) Updated ISP function procedure Updated Package Drawing |
| 0.21 | Mar 10, 2017 | Added Table 5, I ² C Electrical Characteristics |
| 0.22 | Oct 11, 2017 | Fixed I ² C Timing diagram on page 12 to show output disabled when first PFM value is written. Added Output Drive Strength Control to Block Diagram on page 9 Changed PFM Range from 12.59 - 16.34 to 13.83 – 15.43. Changed 156.25 MHz programming example so that it corresponds to the new PFM range. Updated logo and company address, other page layout changes |
| 0.90 | Apr 2, 2018 | Preliminary release |
| 0.91 | Apr 25, 2020 | ±10 ppm option Updated POD (Dimensions Drawings) Corrected I2C typo for read and write bit polarity Fixed Tables 13 and 14 typos by swapping MISO and SS bar pins Updated mechanical shock resistance to 10k g Updated jitter Added Evaluation and Demo Boards reference in Additional Information Other page layout changes Added HTS classification code Added 105°C support for I2C operation Increased max operating junction temperature for 70°C and 85°C ambient Updated Section 8 frequency programming example Clarified HCSL frequency support in Table 2 and Ordering Information section Updated I2C Timing Requirements for "Fall time of both SCLK and SDA" |
| 1.0 | Nov 4, 2020 | Updated I ² C Write/Read Sequence section Updated schematics Updated frequency re-programming section Updated register description section Removed HCSL maximum output current specification Changed rev table date format Final release |
| 1.01 | 30-Apr-2021 | Updated Table 17 Updated hyperlink to Manufacturing Notes; Changed date format |

SiTime Corporation, 5451 Patrick Henry Drive, Santa Clara, CA 95054, USA | **Phone:** +1-408-328-4400 | **Fax:** +1-408-328-4439

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